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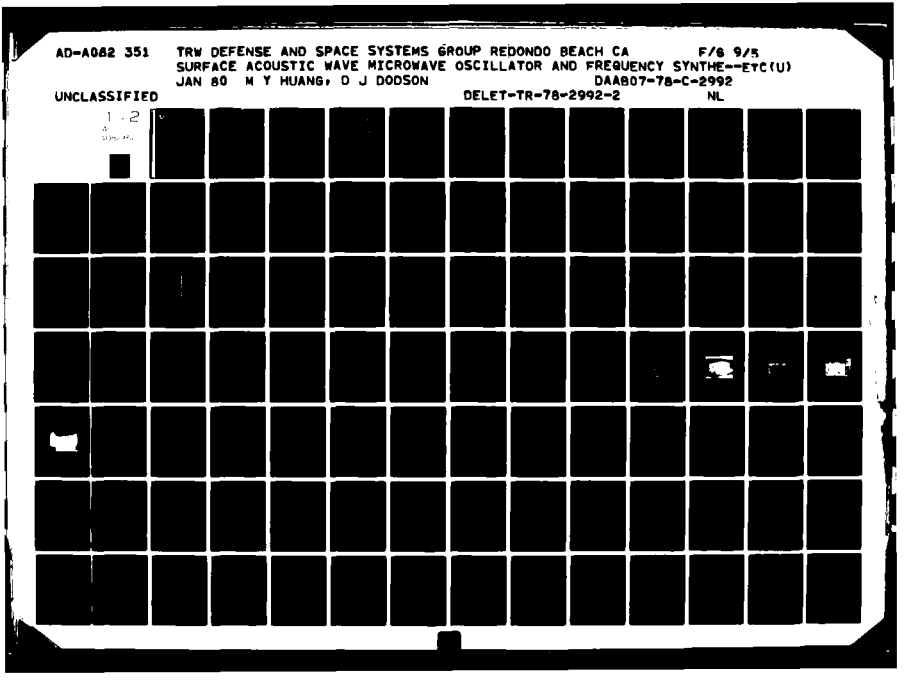

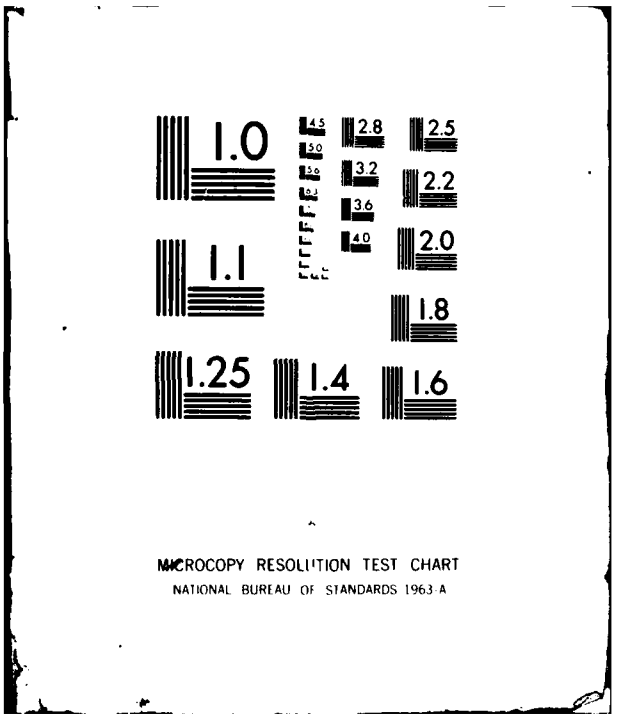
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RESEARCH AND DEVELOPMENT TECHNICAL REPORT
DELET-TR-78-2992-2

SURFACE ACOUSTIC WAVE MICROWAVE OSCILLATOR AND FREQUENCY SYNTHESIZER

D. J. Dodson, Jr., M. Y. Huang
TRW Inc
One Space Park
Redondo Beach, CA 90278

January 1980

Second Interim Report for Period 1 Apr 1979 - 1 Oct 1979

Approved for Public Release;
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Prepared for:
ELECTRONICS TECHNOLOGY & DEVICES LABORATORY

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SAW Synthesizer
SAW Bandpass Filters

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The objective of the program is the development of Surface Acoustic Wave (SAW) oscillator and synthesizer technology. The two year effort is planned as follows: Task I - Development of SAW devices for oscillator applications at microwave (L-band) frequencies. Emphasis to be placed on achieving wideband tuning capabilities, improved oscillator stability performance and reduced power requirements. Task II - Investigate UHF surface acoustic wave devices which can best impact on synthesizer performance parameters such as: switching speed, →

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minimum frequency step size, total achievable bandwidth, short, medium and long term stability as well as maximum suppressionof spurious mode level. Concurrently promising new synthesizer designs will be studied on the basis of these designs to arrive at target specification in a package providing a significant reduction in size, weight and power consumption.

During the second six months of the program, the microwave oscillator design has been completed. A breadboard version of the circuit has been fabricated and is being evaluated. The oscillator design consists of a bank of four selectable SAW delay lines with passbands around 560 MHz, a varactor tuned quadrature hybrid phase shifter, a three stage loop amplifier, a transistor frequency tripler, and a power amplifier. An injection locked oscillator has also been developed to use in place of the power amplifier. An effort has been made to use distributed circuitry through out to minimize parts and assembly costs. The use of a varactor tuned phase shifter is a deviation from the design reported earlier. The varactors have replaced tunable capacitors, and offer the advantage of providing single point tuning and FM capability. Temperature stability of the varactor tuned circuit is inferior to that of the capacitor circuit. A compensation network was incorporated.

Work on the frequency synthesizer was also initiated during this six month period. A number of potential synthesizer architectures were identified and compared. The baseline architecture consists of a bank of independent, injection locked, SAW oscillators providing the fundamental synthesizer frequencies of 486, 526.5, 567 and 607.5 MHz. These tones are filtered in a SAW filter bank and used to drive a mix and divide Synthesizer Module. The output of the Synthesizer Module is frequency doubled and amplified in an Output Module. The Synthesizer Module consists of four RF/LSI SP3T switches and four RF/LSI mix and divide circuits. Design of the SP3T switch is complete. Work on the mix and divide circuitry is in progress.

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1. SUMMARY

The objectives of this program are to develop SAW devices suitable for use in a low cost, stable, .5 watt, 1680 MHz SAW oscillator and an L-band frequency synthesizer suitable for use in JTIDS Class 3 type terminals. One year after contract start, the SAW stabilized oscillator effort has concluded, while the synthesizer architecture is finished and hardware development of the key building blocks is well underway. This second interim technical report will discuss the technical progress in fulfilling contract objectives, the various problems encountered, proposed solutions, and areas for further development to realize the full potential of the designs employed. Section 2 discusses the oscillator, while the synthesizer is discussed in Section 3.

2. MICROWAVE OSCILLATOR

The goal of the microwave oscillator program is a .5 watt output, SAW stabilized circuit which can be frequency and amplitude modulated. The oscillator is to have its center frequency at 1680 MHz, be tunable over a $\pm$20 MHz range, and operate over relatively severe environmental conditions. Table 2-1 summarizes the key requirements of this oscillator.

Figure 2-1 shows a block diagram of the oscillator configuration which provided the best results. It consists of a SAW oscillator operating at 1/3 of the output frequency. The output of this circuit is tripled and then amplified to the desired output power. Two options exist to provide the amplification: a Class C power amplifier and an injection locked oscillator. Both approaches are being investigated.

Table 2-1. OSCILLATOR REQUIREMENTS AND CAPABILITIES

Item No.	Parameter	Requirement	Capability BB #1	Comment	Capability BB #2	Comment
1	Frequency	1660-1700 MHz	1660-1698 MHz	Figs. 2-33, 2-36, 2-39, 2-42	1660-1696 MHz	Figs. 2-45, 2-48 2-51, 2-54
2	Frequency Settability	±250 KHz	≤50 KHz	≤20 KHz Typ.	≤50 KHz	≤20 KHz Typ.
3	Temperature Stability	<200 ppm (-70°C - +70°C)	214-257 ppm	Table 2-3	159-501 ppm	Table 2-8
4	Output Power	.5W (+27 dBm)	+28 dBm Typ.	Table 2-3	+27.9 dBm Typ.	Table 2-8
5	Modulation Capacity					
	FM	>300 KHz/Vrms sensitivity	1.2 MHz/Vrms Typ.		1.2 MHz/Vrms Typ.	
	AM	Pulsed	Pulsed		Pulsed	
6	DC Power	2.5W	3.42W Nom.	Table 2-2	3.50W Nom.	Table 2-6

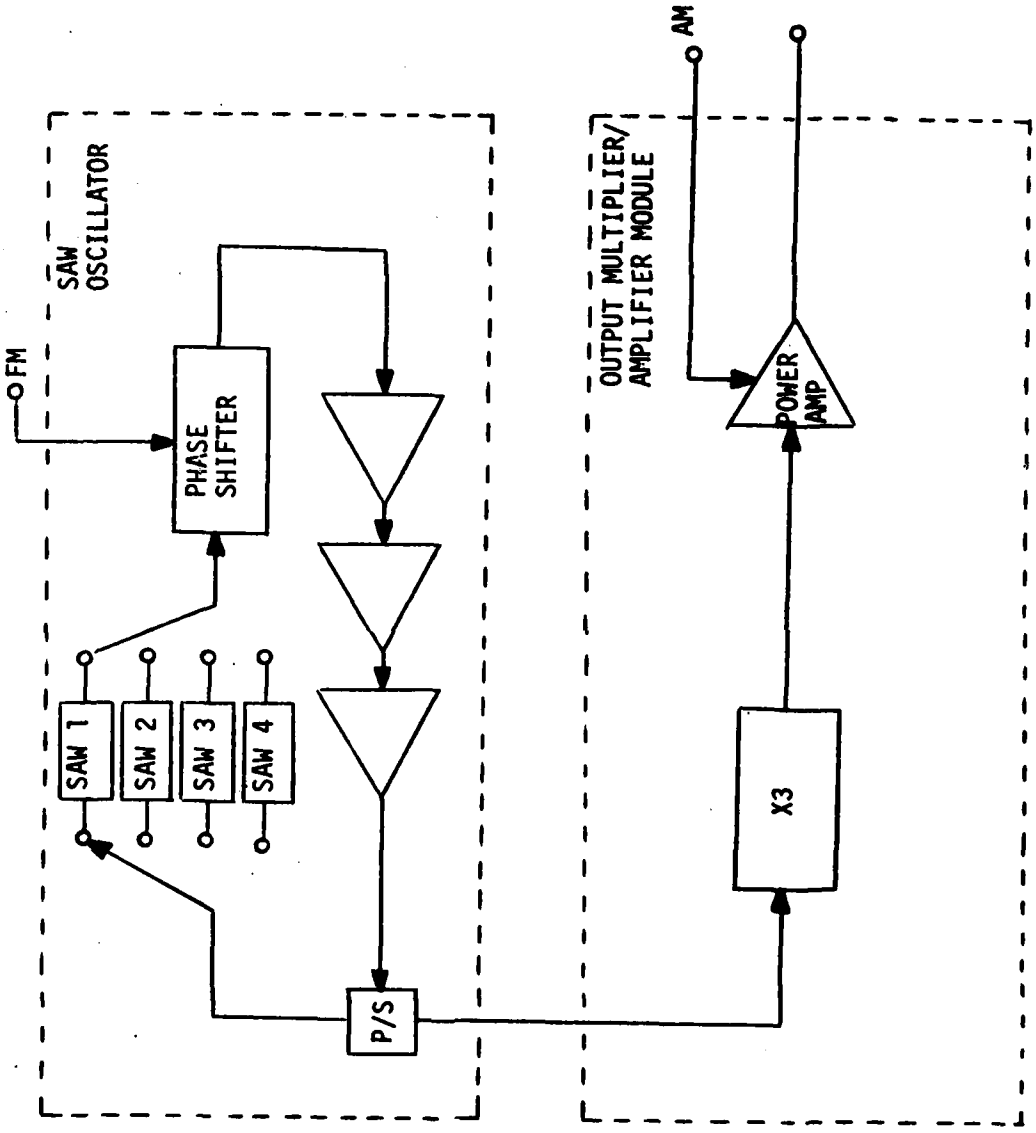


Figure 2-1. OSCILLATOR BLOCK DIAGRAM

The 560 MHz SAW oscillator is achieved by selecting one of four SAW delay lines. These filters cover the range from $555\frac{1}{3}$ to $556\frac{2}{3}$ MHz, $556\frac{2}{3}$ to 560 MHz, 560 to $563\frac{1}{3}$ MHz, and $563\frac{1}{3}$ to $566\frac{2}{3}$ MHz. These SAW filters are cascaded with the phase shifter which is used to tune to any frequency within the passband of the selected SAW filter. A three stage amplifier provides the gain to overcome the filter and phase shifter insertion losses and the closed loop configuration oscillates at a frequency in which the total phase shift around the loop is a multiple of 2π. The two conditions for oscillation can be expressed as:

$$\frac{2\pi f_n \ell}{V} + \phi = 2n\pi \qquad (2\text{-}1)$$

and

$$L_S(f) + L_I(f) = G(f,A) \quad , \qquad (2\text{-}2)$$

where f_n = oscillation frequencies

ℓ = center-to-center transducer separation

V = surface wave velocity

ϕ = phase shift through all elements except SAW delay line

n = an integer

$L_S(f)$ = insertion loss of SAW delay line

$L_I(f)$ = insertion loss of feedback loop components

$G(f,A)$ = amplifier gain as a function of f and output level, A

A = output power level .

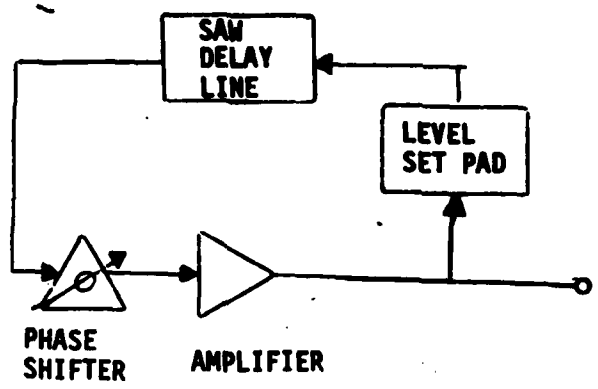


Figure 2-2. SAW Oscillator Configuration.

Solving (2-1) for f_n,

$$f_n = \frac{V}{\ell}(n - \frac{\phi}{2\pi}) \quad . \qquad (2\text{-}3)$$

For single mode operation, the SAW delay line is designed such that there is only one solution for Equation (2-1) that is in the passband of the delay line. As a general rule, the loss associated with the feedback loop components, $L_I(f)$, and the amplifier gain, $G(f,A)$, are slowly varying functions of frequency over a broad range around the frequency for which the oscillator is being designed, and the SAW response, $L_S(f)$, is a very strong function of frequency. The SAW oscillator is designed so that the combination of SAW delay line loss plus amplifier gain exceeds unity over a desired frequency band around the desired operating frequency. As long as only one solution to (2-3) falls within the passband response of the SAW delay line, single mode operation of the SAW oscillator is guaranteed.

The phase shifter consists of a quadrature hybrid which produces phase shift when its load impedance is changed. Varactor diodes resonated with shorted stubs are used for the reactive loads of the quadrature hybrid. Two such circuits are used in the current design, although an improved advanced development version should operate satisfactorily with only one phase shifter. FM modulation is achieved by applying the modulating signal to the varactor diodes. Pulse AM modulation is achieved by modulating the bias of the tripler circuit.

a. SAW Delay Line Design

As mentioned above, the 560 MHz SAW oscillator is achieved by selecting one of four SAW filters which cover the range from 553-1/3 to 556-2/3 MHz, 556-2/3 to 560 MHz, 560 to 563-1/3 MHz, and 563-1/3 to 566-2/3 MHz. The SAW delay line is designed to achieve the required passband frequencies and delay times while maintaining a minimum insertion loss and good temperature stability. The delay time is important since it directly determines the mode spacing and thus the tuning range of the SAW oscillator.

The rationale for segmenting the passband into four sub-bands is as follows: The delay line bandwidth or tunability range of a SAW delay line is inversely proportional to its time delay and oscillator Q. In order to achieve a single mode frequency selectability from 1660 to 1700 MHz, a $\pm$12000 ppm frequency band, the center separation between the input and output transducers must be less than 50 λ_0. This sort of separation creates two problems. First, the direct feedthrough can enhance the delay time sidelobe levels and if there is sufficient excess gain in the loop will allow more than one mode to oscillate. Secondly, the delay line insertion loss becomes excessive due to the limited number of finger pairs in the transducer.

A delay line on ST-cut quartz with 40 λ_0 transducer separation was projected to have insertion loss in excess of 40 dB. To reduce this large loss it was decided to divide the 1660 to 1700 MHz frequency range into several channels. By a trade-off analysis considering insertion loss, sidelobe rejection, circuit complexity, and yield, we settled on four channels as the optimum choice.

With the number of channels optimized, the choice of the SAW delay line frequency was considered. Frequencies to be considered include the fundamental oscillator frequency and the various subharmonics. With the present state of the art, it is extremely difficult, if not impossible, to mass produce SAW delay lines operating at the fundamental. Either an embedded transducer finger configuration or an extremely thin interdigital finger metallization layer (200Å) would have to be employed if mode conversion at the surface discontinuities are to be minimized and to assure insertion losses of less than 30 dB. Even using these techniques, the typical variation of delay line frequency due to fabrication tolerance is estimated to be $\pm$10 MHz, too large to be of practical use.

Design of the delay line at a subharmonic of 1680 MHz appears a more practical approach for a circuit requiring mass production. Both one-half and one-third output frequencies were considered. Delay lines operating at the one-half frequency can be produced using photolithographic techniques, however, center frequency reproducibility and insertion loss are not easily controlled. Again, this is mainly due to fabrication tolerances and mode conversion which could be improved by using embedded transducers or very thin electrode metallization as mentioned previously, but both of these approaches would lead to increased SAW production costs.

These production problems can be alleviated by lowering the delay line frequency as in this case to the third subharmonic. The device design would be similar to a one half frequency design but with increased line widths. Hence, four delay lines with center frequencies at 555 MHz, 558-1/3 MHz, and 565 MHz were designed on a single substrate. Each of the delay lines consists of two identical interdigital transducers with split electrode configuration. The choice of identical transducer design minimizes or eliminates fabrication errors that can cause the passbands of input and output transducers to differ, resulting in an increase in insertion loss. The split electrode configuration allows the delay line to operate at the 3rd harmonic so that linewidth resolution for the fingers stays above 2.2 μm. This linewidth can be easily fabricated in quantity using conventional photolithographic techniques.

The center-to-center separation between the input and output transducers determines the time delay for the SAW delay line. The time delay then limits the length of the transducer, which in turn gives a lower bound for the delay line bandwidth. On the other hand, the mode-spacing and the tuning range is inversely proportional to the time delay and to ensure wide tuning range and single mode operation, the transducers have to be placed very close to one another and contain the maximum allowable finger pairs. For the present design, this center-to-center separation was set at 98 λ_o, where λ_o is the acoustic wavelength at the center frequency of each delay line. The transducers each consist of 29 finger pairs, and the edge-to-edge separation between transducers is only 10 μm. Fortunately, it was found that with proper packaging, the direct electromagnetic feedthrough at this separation can still be suppressed to below 20 dB of the passband peak. The acoustic aperture for these delay lines was designed to be 200 λ_o.

With the above design, the SAW delay line oscillator achieves single mode operation and the oscillator frequency can be tuned to the required frequencies using a phase shifter capable of $\pm$ 100° phase tuning. The untuned insertion loss of the delay line is 30 dB, which after tuning becomes less than 23 dB.

In the course of fabricating the delay lines for the first prototype oscillator a significant problem was encountered. Impedance and phase variation measurements among the four segmented bandwidths were found to be non-uniform and staggered, respectively. This in effect required a different set of matching networks for each line and an electrical phase shifting capability in excess of the designed for $\pm$110° phase capability if one phase shifter was to provide tuning across all four segmented bands. Since time under this program did not permit a redesign, two phase shifters were implemented in the deliverable units so that 360° of phase shift could be achieved.

The problem of reproducibiltiy of the SAW filter response needs to be addressed in subsequent work. The phase shifts experienced are really very small in terms of wave lengths of the surface acoustic wave, but have dramatic impact on the oscillator performance. Even though the same SAW mask was used, it was felt that the combined effects of metallization thickness of the SAW tranducers and the variation in crystal characteristics was sufficient to cause this undesired phase shift.

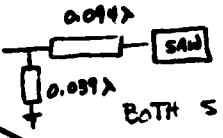
Figure 2-3 is a plot of the input and output reflection coefficient of one SAW filter in breadboard unit 1. The forward transmission magnitude and phase of all four delay lines of unit 1 are shown in Figures 2-4 through 2-7. Figure 2-8 is a schematic of the matching network for these SAW filters. Note that a completely distributed matching network is used to ease producibility and minimize adjustment costs during production. In fact, its advantage of not requiring tuning might be its downfall if repeatable SAW filter characteristics cannot be achieved.

(14)

NAME M. BRUNSMAN	TITLE SAW #2 F1 CHANNEL	DWG. NO.
SMITH CHART FORM 82-BSPR(9-65)	KAY ELECTRIC COMPANY, PINE BROOK, N.J. © 1966. PRINTED IN U.S.A.	DATE 11/27/79

Blue = OUTPUT
Black = INPUT
SAW: 2, F1 CHANNEL

IMPEDANCE OR ADMITTANCE COORDINATES



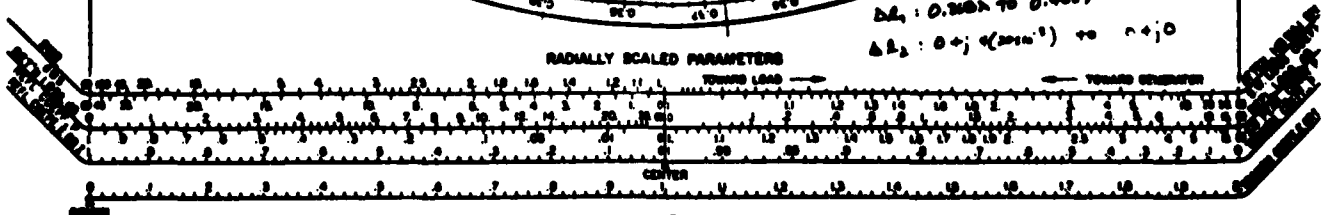
BOTH SIDES

R_1 was : 0.083λ
R_2 was : 0.20?λ

ΔL_1 = 0.094λ
ΔL_2 = 0.03?94λ

Figure 2-3
SAW REFLECTION
COEFFICIENT

ΔL_1 : 0.?83λ TO 0.468λ
ΔL_2 : 0 + j ∞(2π tan⁻¹) TO ∞ + j0



A MEDA-CHART

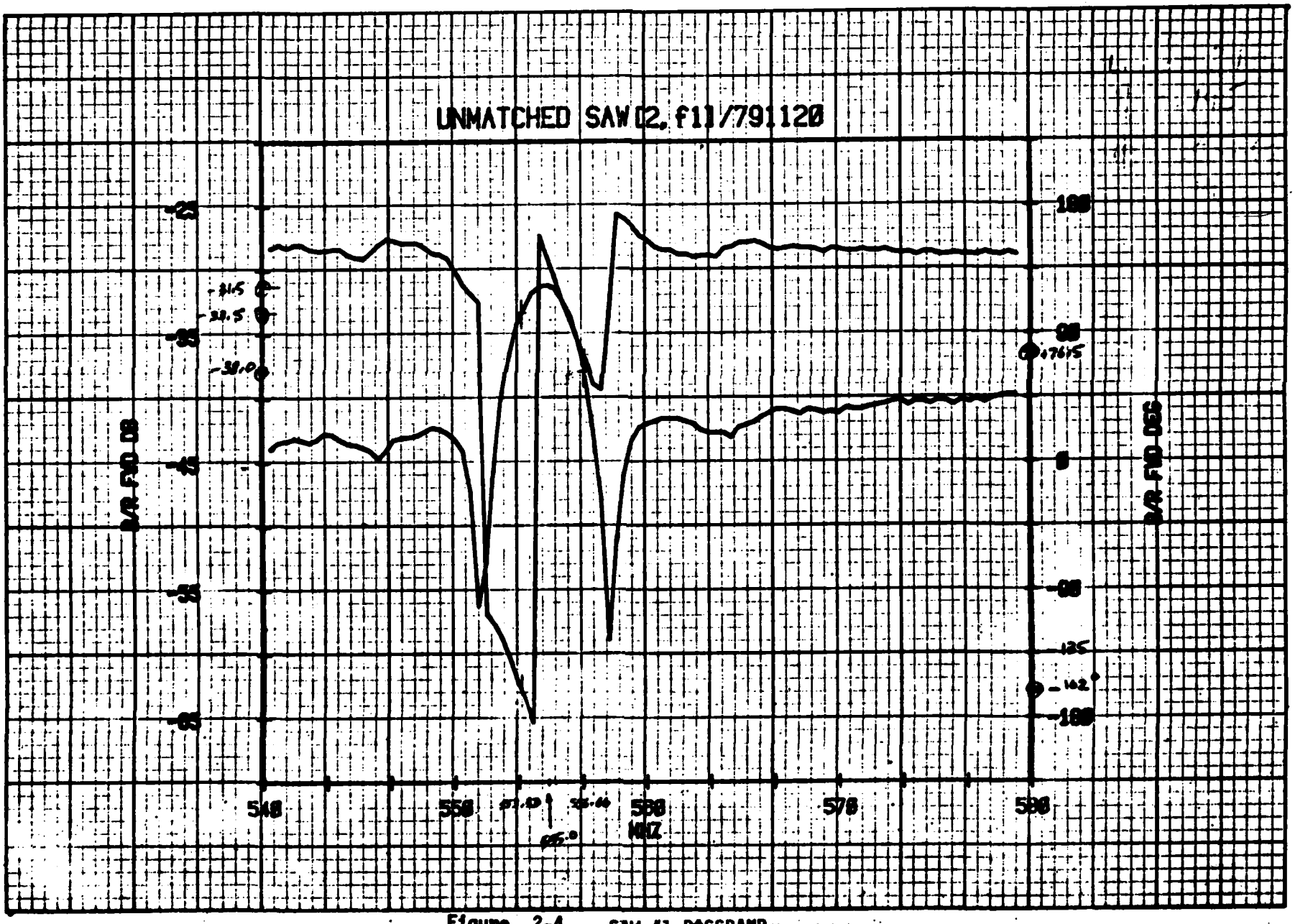


Figure 2-4 SAW #1 PASSBAND

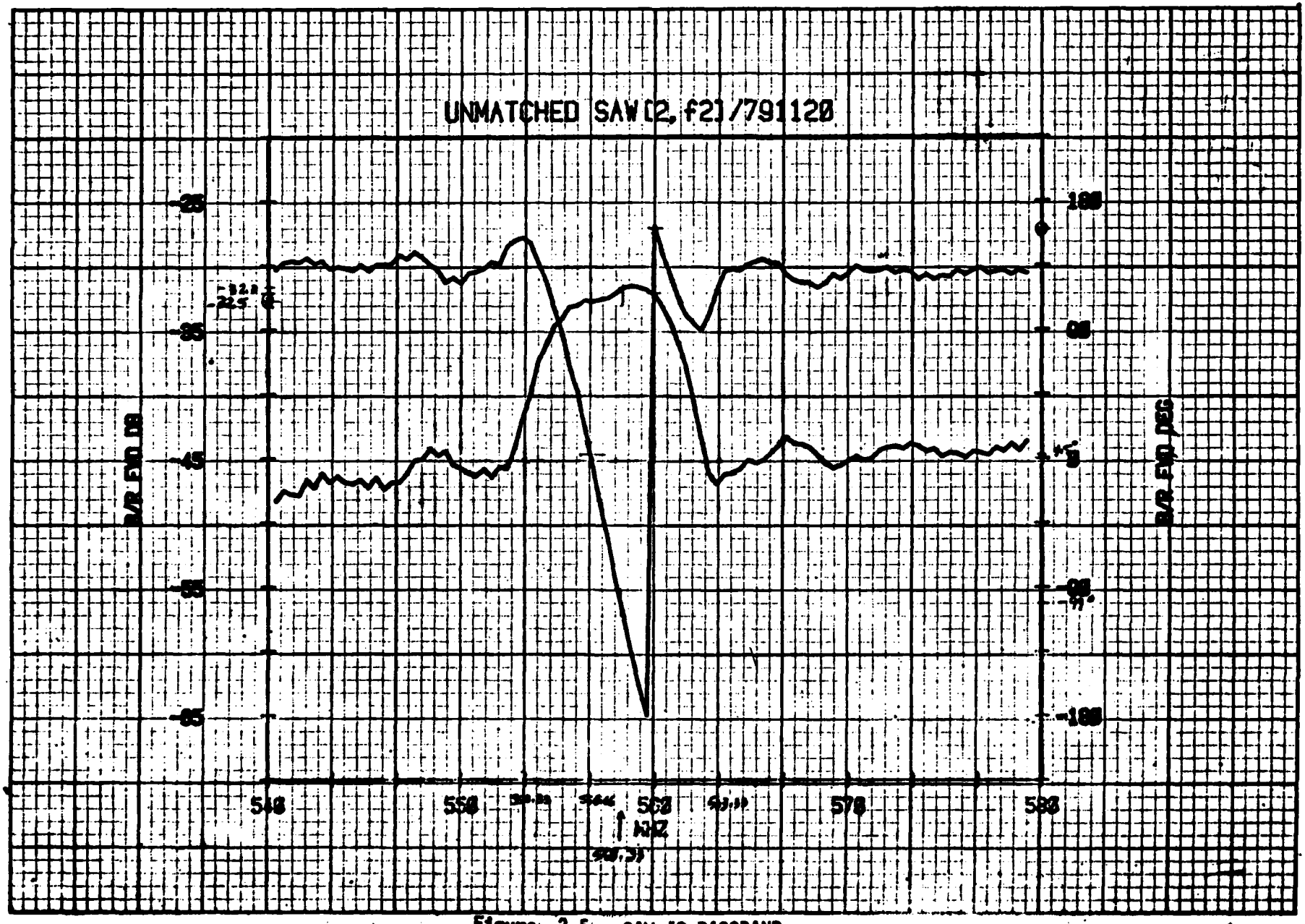


Figure 2-5 SAW #2 PASSBAND

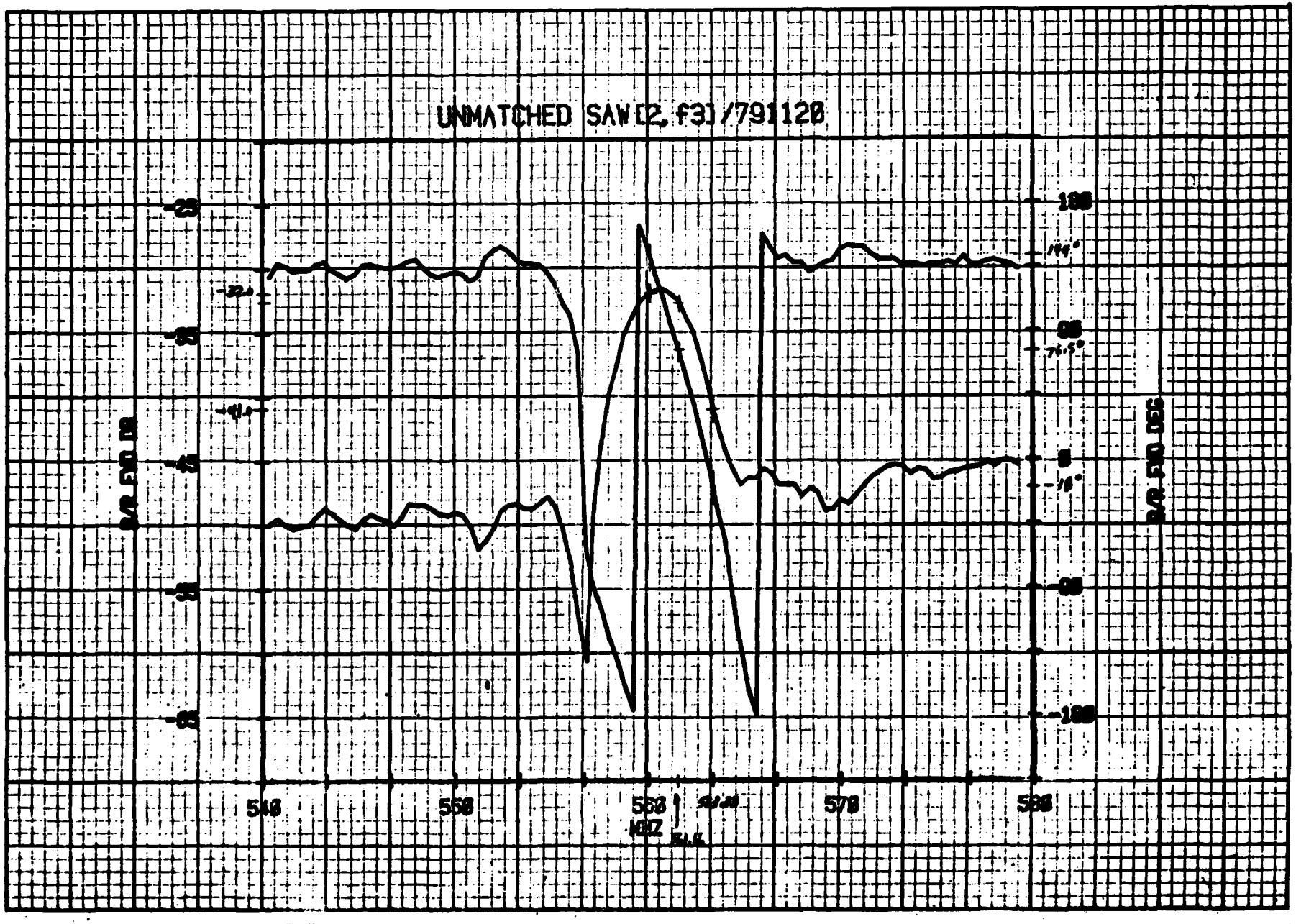


Figure 2-6 SAW #3 PASSBAND

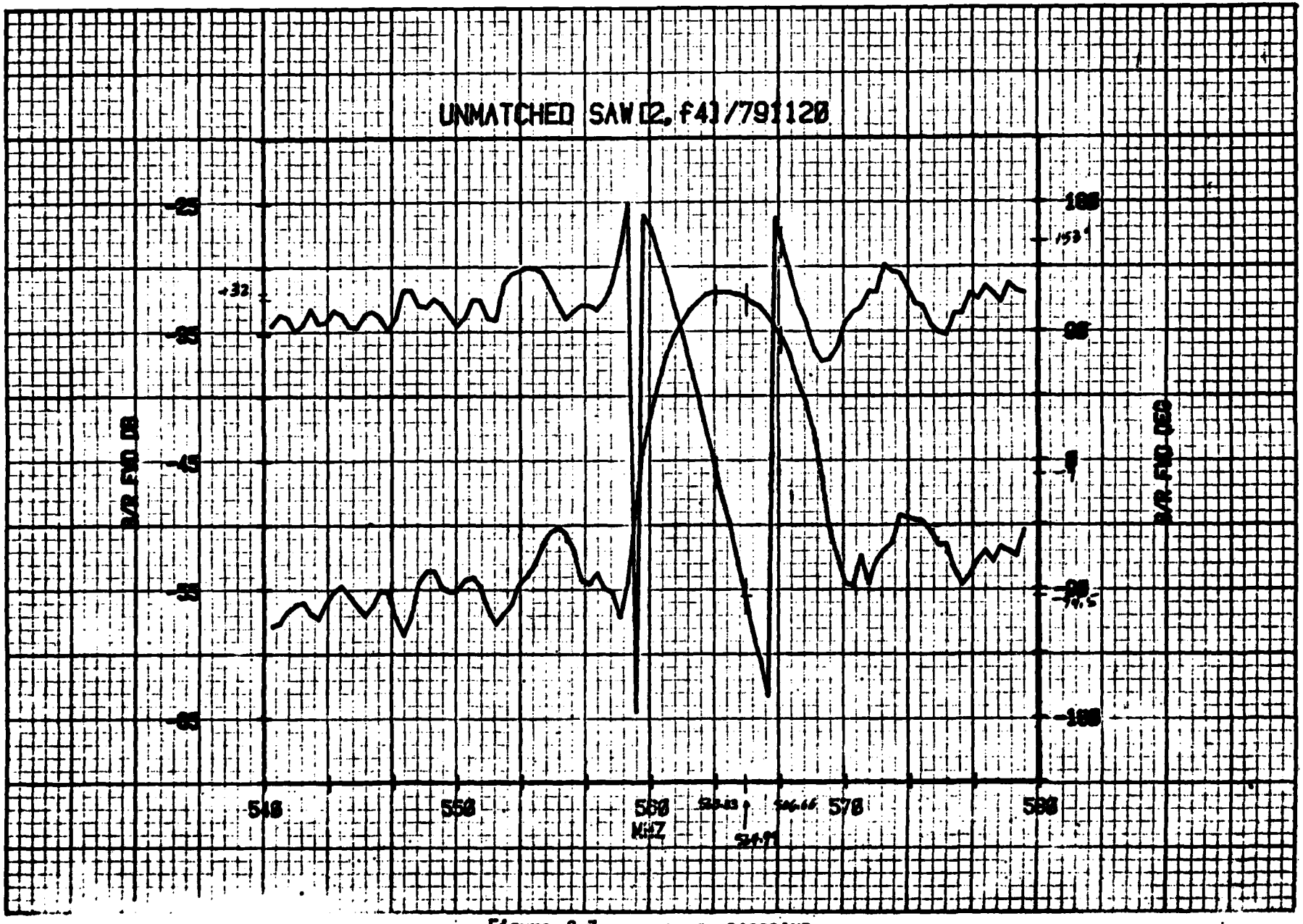


Figure 2-7 SAW #4 PASSBAND

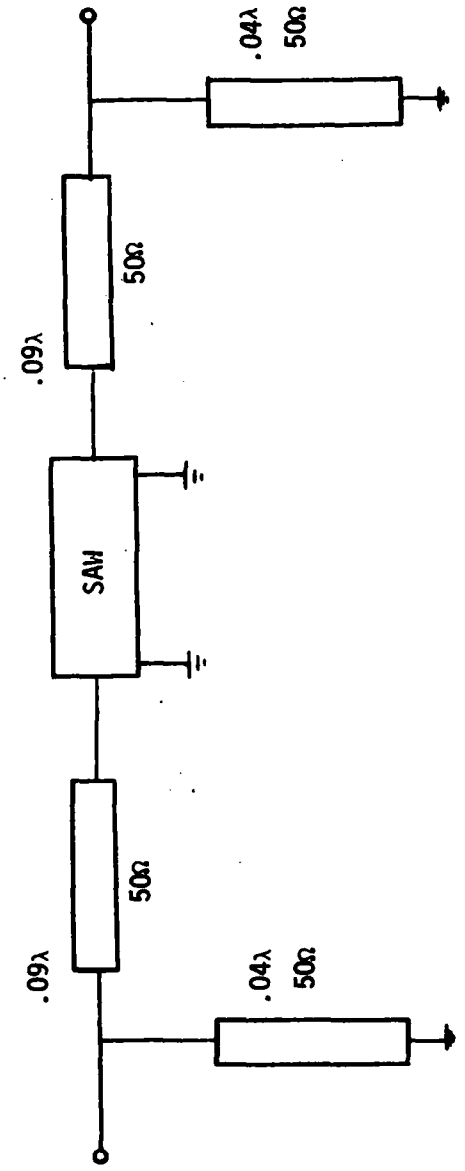


Figure 2-8 SAW Matching Networks

b. Electrical Design

(1) Phase Shifter

The phase shifter forms a key part of the microwave oscillator since by tuning the phase the desired frequency of oscillation can be selected. The design selected for the phase shifter operates by changing the reflection coefficients of the quadrature hybrid as shown in Figure 2-9.

To operate as a phase shifter, a quadrature hybrid is connected to two reflective networks, one on port 2 and one on port 3. Ports 1 and 4 form the input and output ports, respectively. Let $V_{1in} = Ae^{j\omega t}$ be the signal input to port 1. Then, by the operation of the quadrature hybrid, $V_{2out} = \frac{A}{\sqrt{2}} e^{j\omega t}$ and $V_{3out} = \frac{A}{\sqrt{2}} e^{j(\omega t + \pi/2)}$; i.e., half of the power input to port 1 goes to each of ports 2 and 3, with a 90° phase shift between them. If the networks connected to ports 2 and 3 have reflection coefficients of Γ_1 and Γ_2 respectively, then the signals input to ports 2 and 3 are given as

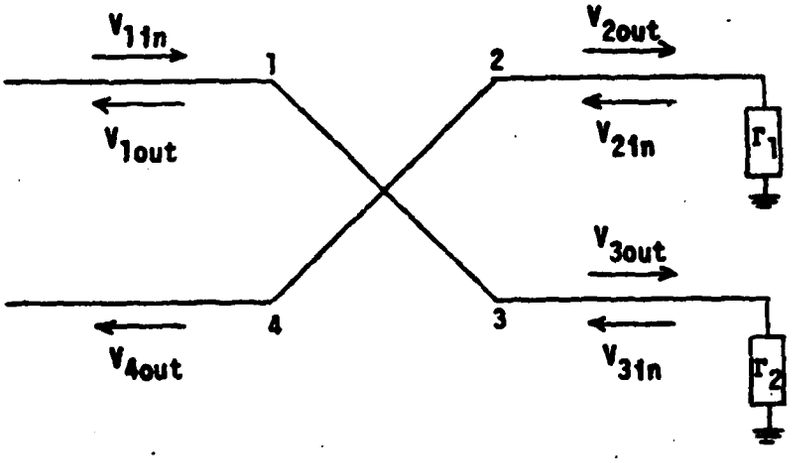


Figure 2-9. QUADRATURE HYBRID PHASE SHIFTER

$$V_{2in} = \frac{A}{\sqrt{2}} e^{j\omega t}\Gamma_1 \tag{2-9}$$

$$V_{3in} = \frac{A}{\sqrt{2}} e^{j(\omega t + \pi/2)}\Gamma_2 \tag{2-10}$$

Then by operation of the quadrature hybrid the power out of ports 1 and 4 is given by

$$V_{1out} = \frac{A}{2} [e^{j\omega t}\Gamma_1 + e^{j(\omega t + \pi)}\Gamma_2] \tag{2-11}$$

$$V_{4out} = \frac{A}{2} [e^{j(\omega t + \pi/2)}\Gamma_1 + e^{j(\omega t + \pi/2)}\Gamma_2] \tag{2-12}$$

It is now apparent that if $\Gamma_1 = \Gamma_2$, then V_{1out} becomes zero and V_{4out} has all the power and a phase shift of $\pi/2 + \angle\Gamma$. But what happens when $\Gamma_1 \neq \Gamma_2$. If we let

$$\Gamma_1 = 1e^{j\phi_1} \tag{2-13}$$

and

$$\Gamma_2 = 1e^{j\phi_2} \tag{2-14}$$

the equation for V_{4out} becomes

$$V_{4out} = \frac{A}{2} [e^{j(\omega t + \pi/2)}e^{j\phi_1} + e^{j(\omega t + \pi/2)}e^{j\phi_2}] \tag{2-15}$$

or

$$V_{4out} = \frac{A}{2} e^{j(\omega t + \pi/2)}(e^{j\phi_1} + e^{j\phi_2}) \tag{2-16}$$

Using trigonometric identities on $e^{j\phi_1} + e^{j\phi_2}$, we find

$$V_{4out} = A \cos \frac{\phi_1 - \phi_2}{2} e^{j(\omega t + \pi/2 + \frac{\phi_1 + \phi_2}{2})} \tag{2-17}$$

Thus the phase shift from port 1 to port 4 is $\pi/2 + \frac{\phi_1 + \phi_2}{2}$. The cosine term tells us that there can be a variation of 90° between ϕ_1 and ϕ_2 before there is 3 dB additional loss when compared to the $\phi_1 = \phi_2$ case.

This wide allowable variation means that the amplitude variation suffered during tuning of the phase shifter can be almost ignored in the design of the oscillator.

By judicious choice of reflective networks, the required phase shift range can be met. A network of a shorted stub with a variable capacitor was chosen for this application. However, it was pointed out that it is difficult to tune both of these capacitors simultaneously, as would be required for optimum performance. Hence, an improved version was attempted in which varactor diodes were used in place of the mechanically tuned capacitors. Initially, high Q diodes mounted in plastic axial lead packages were used for the capacitors, but it was soon discovered that the package parasitics limited the tuning range to only 20° to 50°. This has now been improved to using diodes in pill packages from Microwave Associates and GHz devices. The phase shifter performance is shown in Figure 2-10. We note that the amplitude variation is less than 2 dB and almost 200° of phase shift can be obtained as the tuning voltage is varied from 0 to 24V.

Figures 2-11 and 2-12 are measured plots of phase shift versus voltage taken at -75°C and +70°C. Note the almost linear tuning characteristics obtained by a compensation of the phase shifter design and the capacitance change characteristic of the varactor diode.

Unfortunately, a major problem with the varactor diode is its sensitivity to temperature. Figures 2-13, -14 and -15 are measured plots of the phase shift versus temperature at $555\frac{1}{3}$, 560, and $566\frac{2}{3}$ MHz, respectively. Note that at 20V one obtains almost 10° of phase variation with temperature. Fortunately, it should be relatively straight-forward to temperature compensate this phase shift by using either a thermistor or sensistor. This task will be completed and the temperature compensation incorporated before delivery of the oscillator will be made.

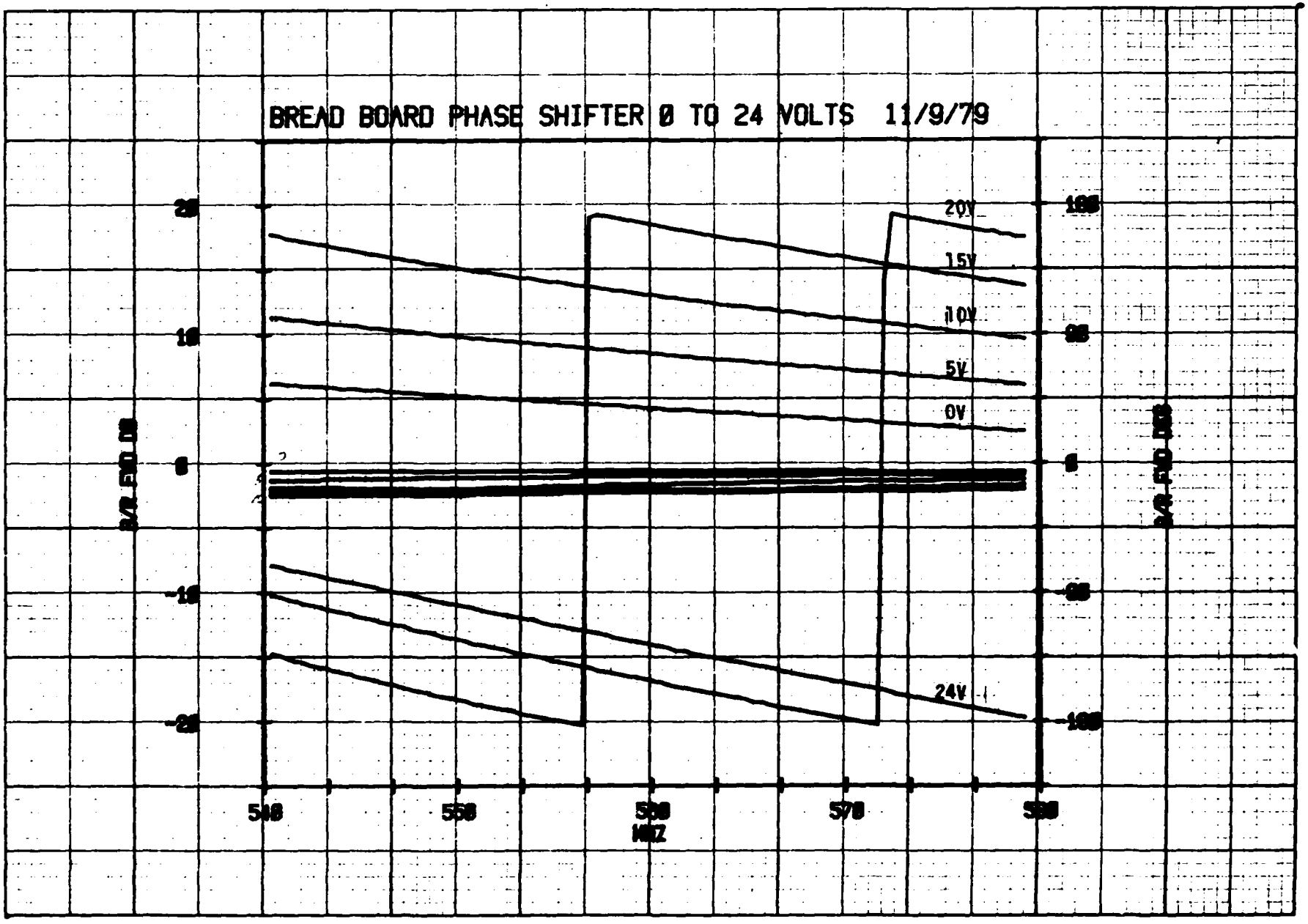


Figure 2-10. BREADBOARD PHASE SHIFTER

Figure 2-11. PHASE SHIFT vs VOLTAGE AT -75°C

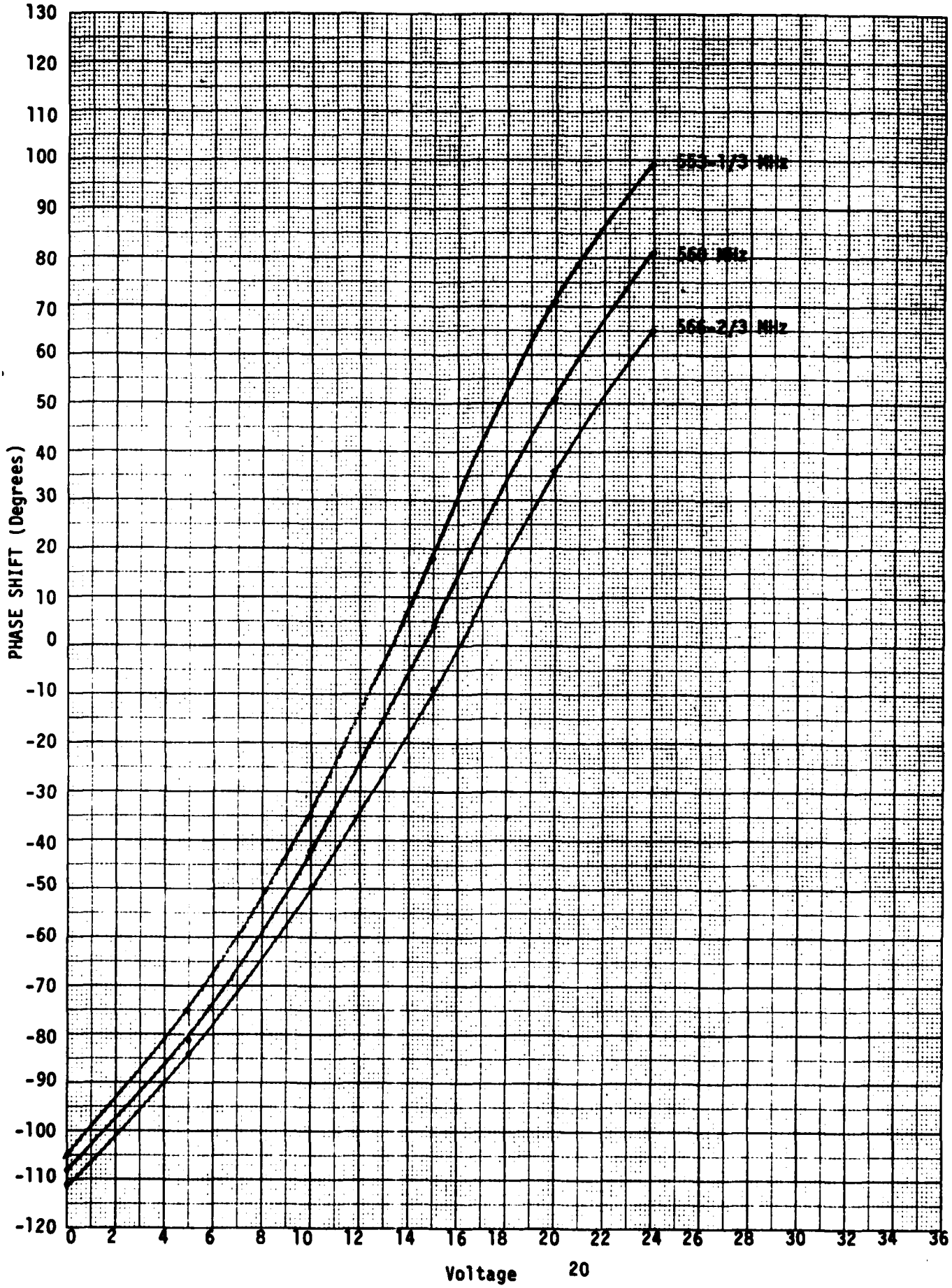


Figure 2-12. PHASE SHIFT vs VOLTAGE AT +70°C

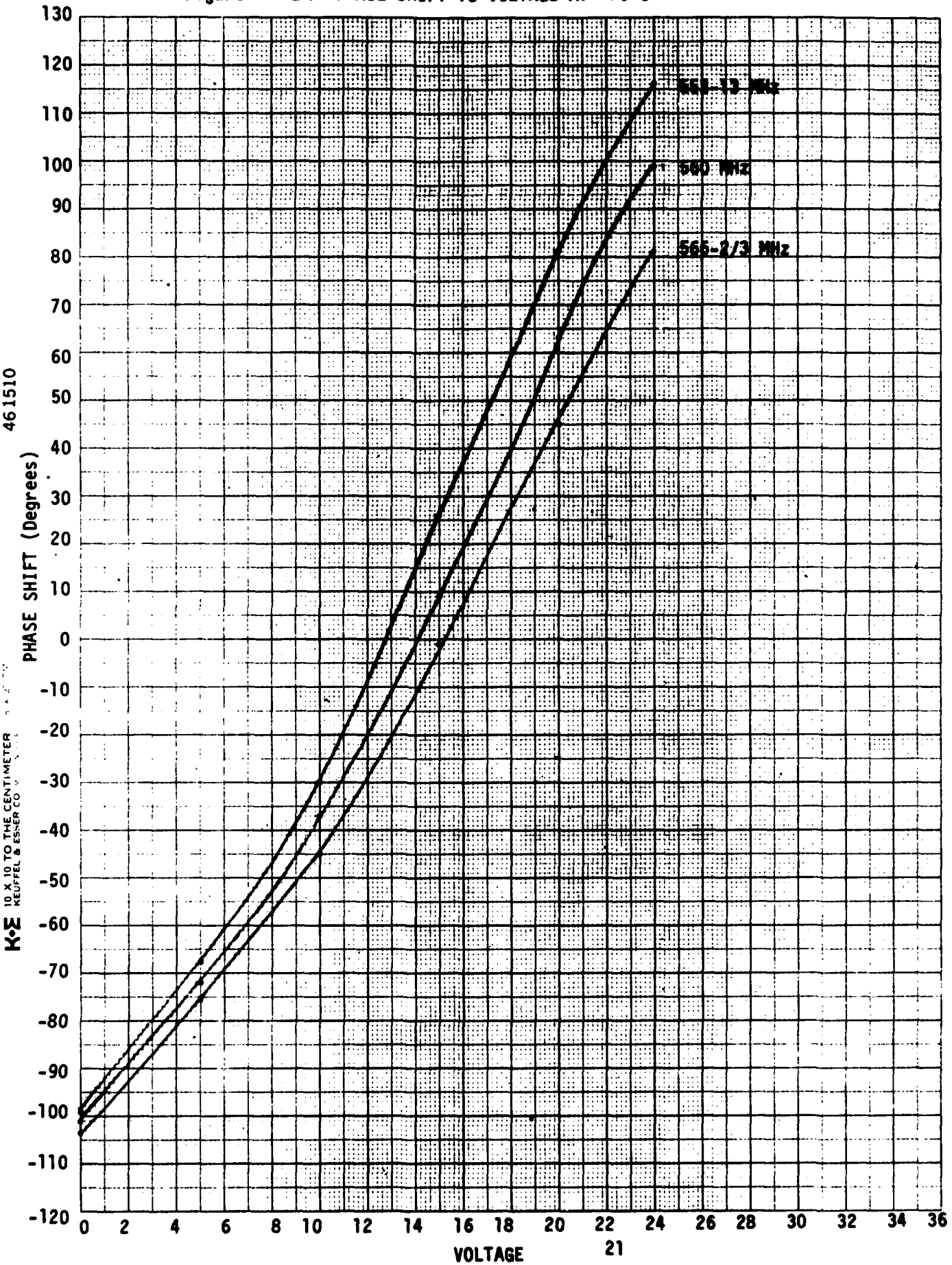


Figure 2-13. PHASE SHIFT vs TEMPERATURE AT 533.33 MHz

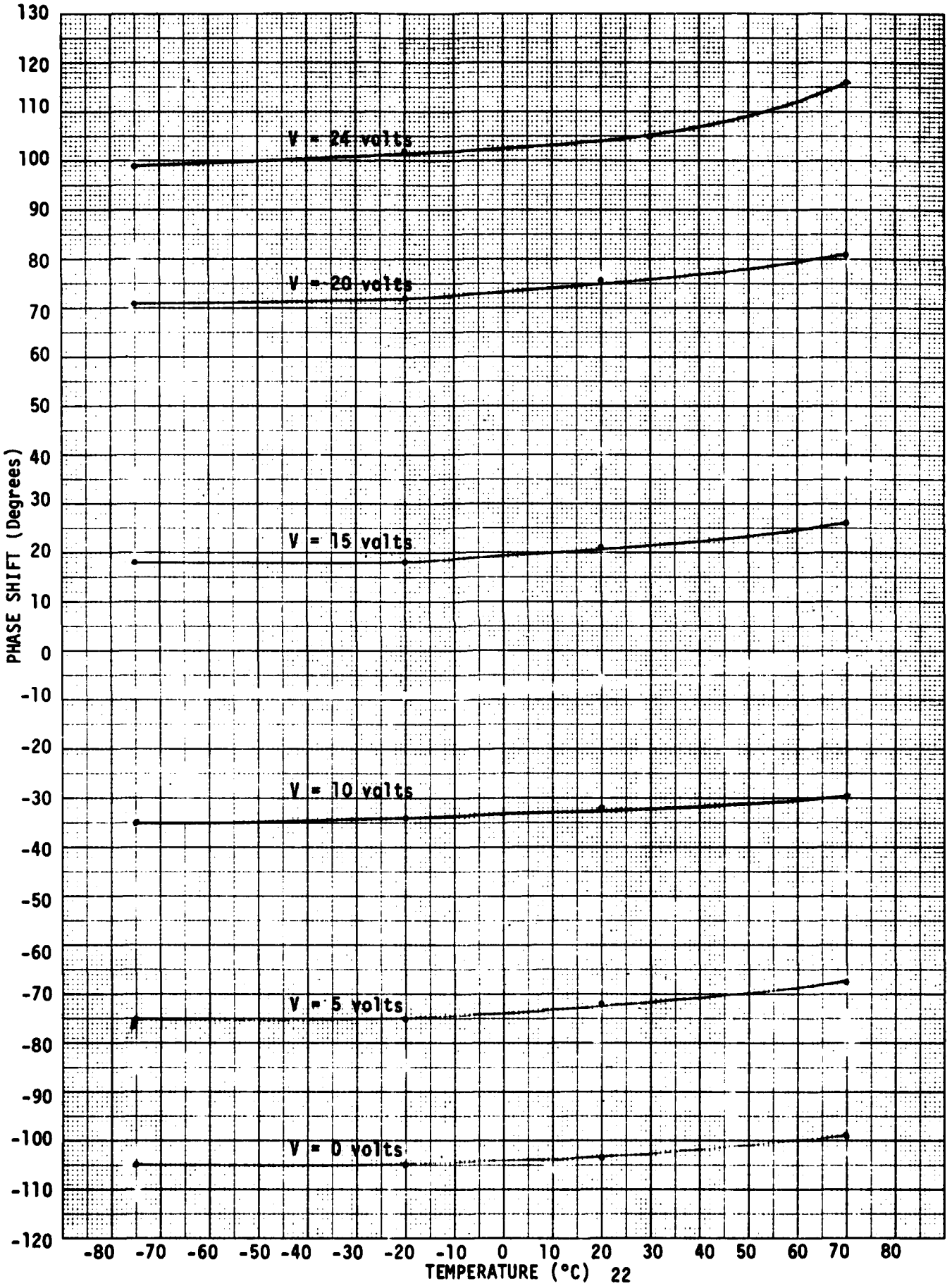


Figure 2-14. PHASE SHIFT vs TEMPERATURE AT 560 MHz

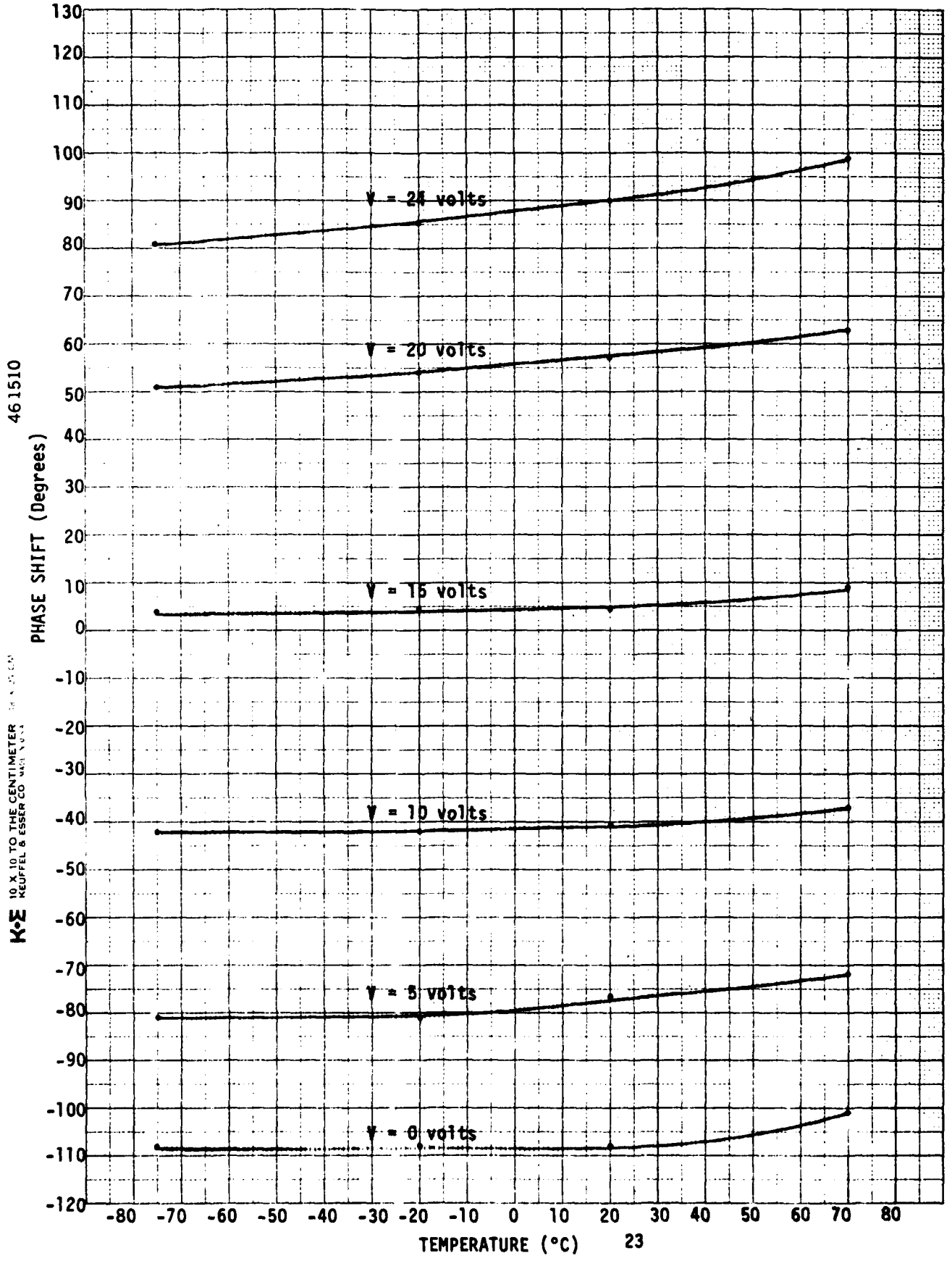
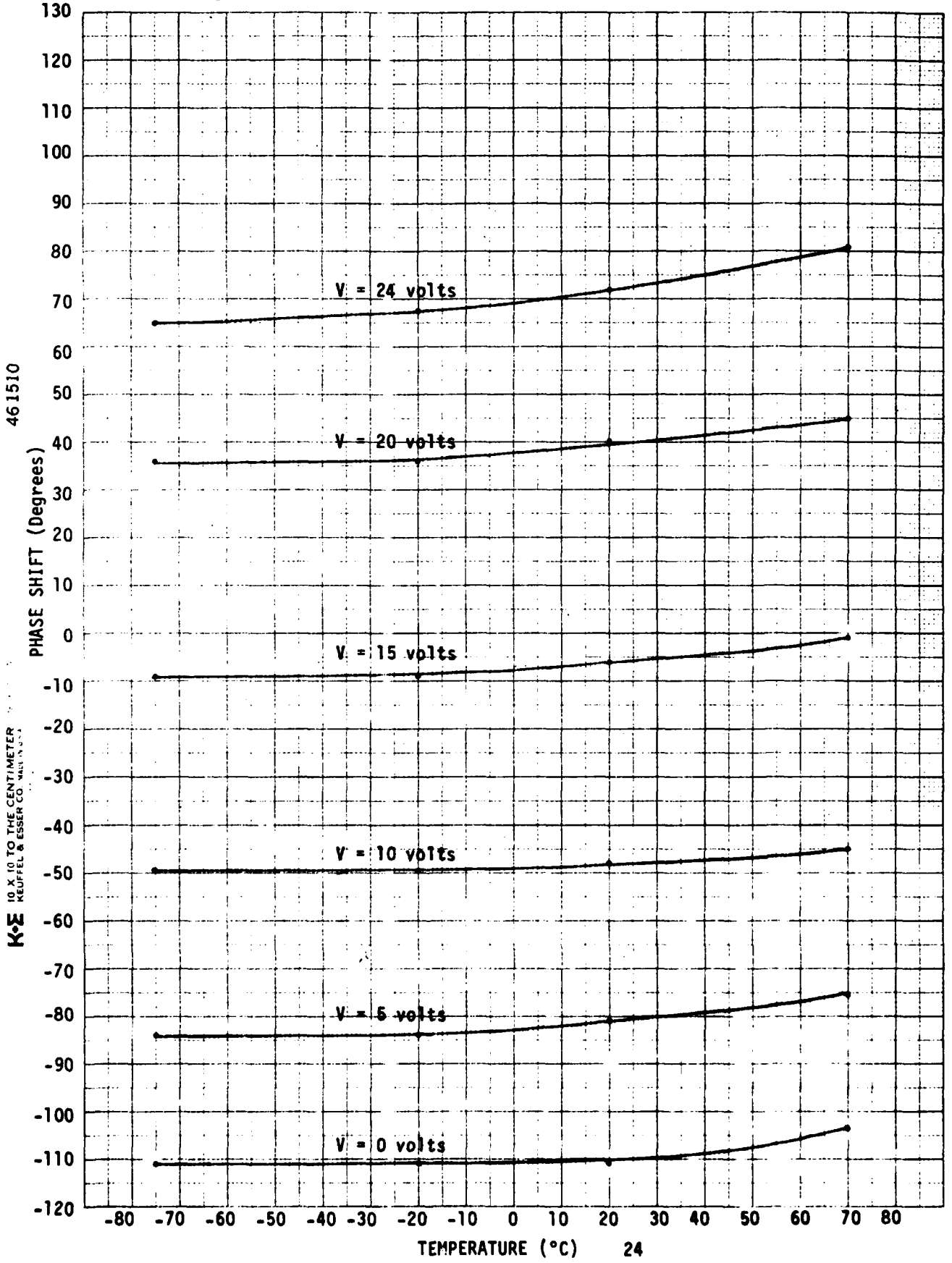


Figure 2-15. PHASE SHIFT vs TEMPERATURE AT 566.66 MHz



One other point needs to be made regarding the use of varactor diodes to achieve the desired phase shift. Because the phase shift is rather sensitive to the biases on the varactors, a well-regulated voltage source is required. Fortunately, since no current is drawn by the diode, the voltage regulation should be easily accomplished with possibly only a zener diode. In fact, it should be possible to design temperature compensation into the regulation circuit.

As mentioned previously, two stages of phase shifters will be cascaded to provide over 360° of phase shift in the deliverable units.

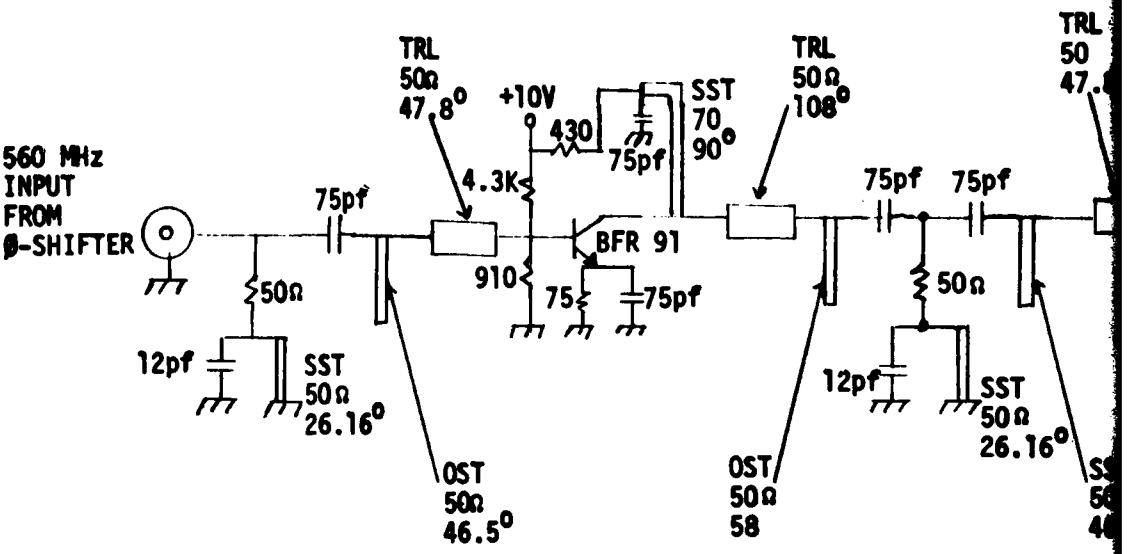
(2) Oscillator Feedback Amplifier

The design of the feedback amplifier is shown in Figure 2-16. This consists of 3 stages of amplification using the Amperex BFR 91 transistor for two stages and the BFR 96 for the output stage. Transistor characteristics are described in the previous semi-annual report and will not be repeated here. Figure 2-17 shows the gain versus frequency of these amplifiers, Figure 2-18 the compression characteristics of the output stage, and Figures 2-19 and 2-20 the matched input and output reflection coefficients. When this amplifier was incorporated with the SAW filters, oscillation was found far out of band (at approximately 170 MHz). This is due to the high reflection coefficient of the SAW filters and the phase conditions set-up in the amplifiers at this frequency. The oscillation problem was solved by sufficiently attenuating the inputs and outputs of the SAW filters to provide an out-of-band quasi-50 ohm load to the amplifiers.

(3) Tripler Design

A schematic of the tripler to multiply the SAW oscillator output to 1680 MHz is shown in Figure 2-21. As will be discussed in Section (4), a tripler is needed regardless of the technique used to amplify the output to .5W. The tripler is a very simple circuit using the BFR 96 transistor.

Figure 2-16. 560 MHz Micro
(Sc



MHz Microwave Oscillator Amplifier Chain
(Schematic)

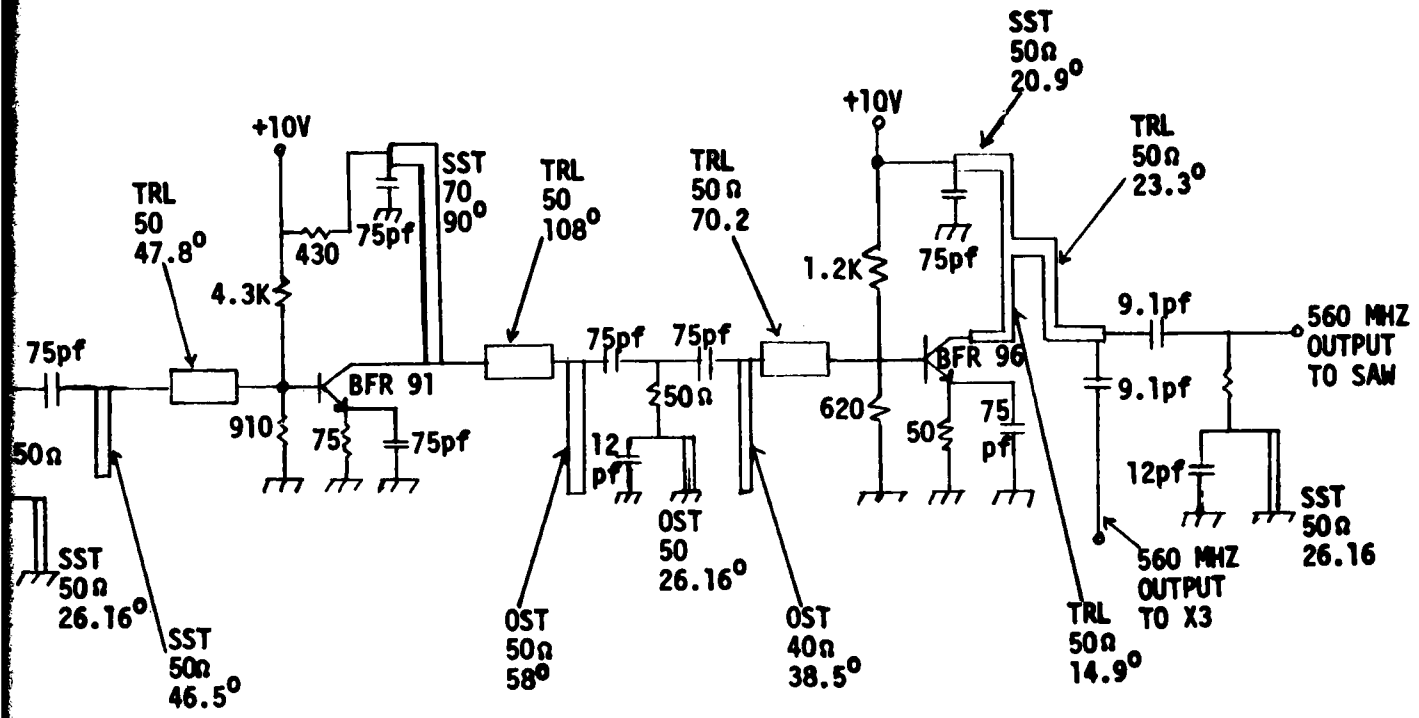


Figure 2-17. AMPLIFIER CHAIN GAIN vs FREQUENCY

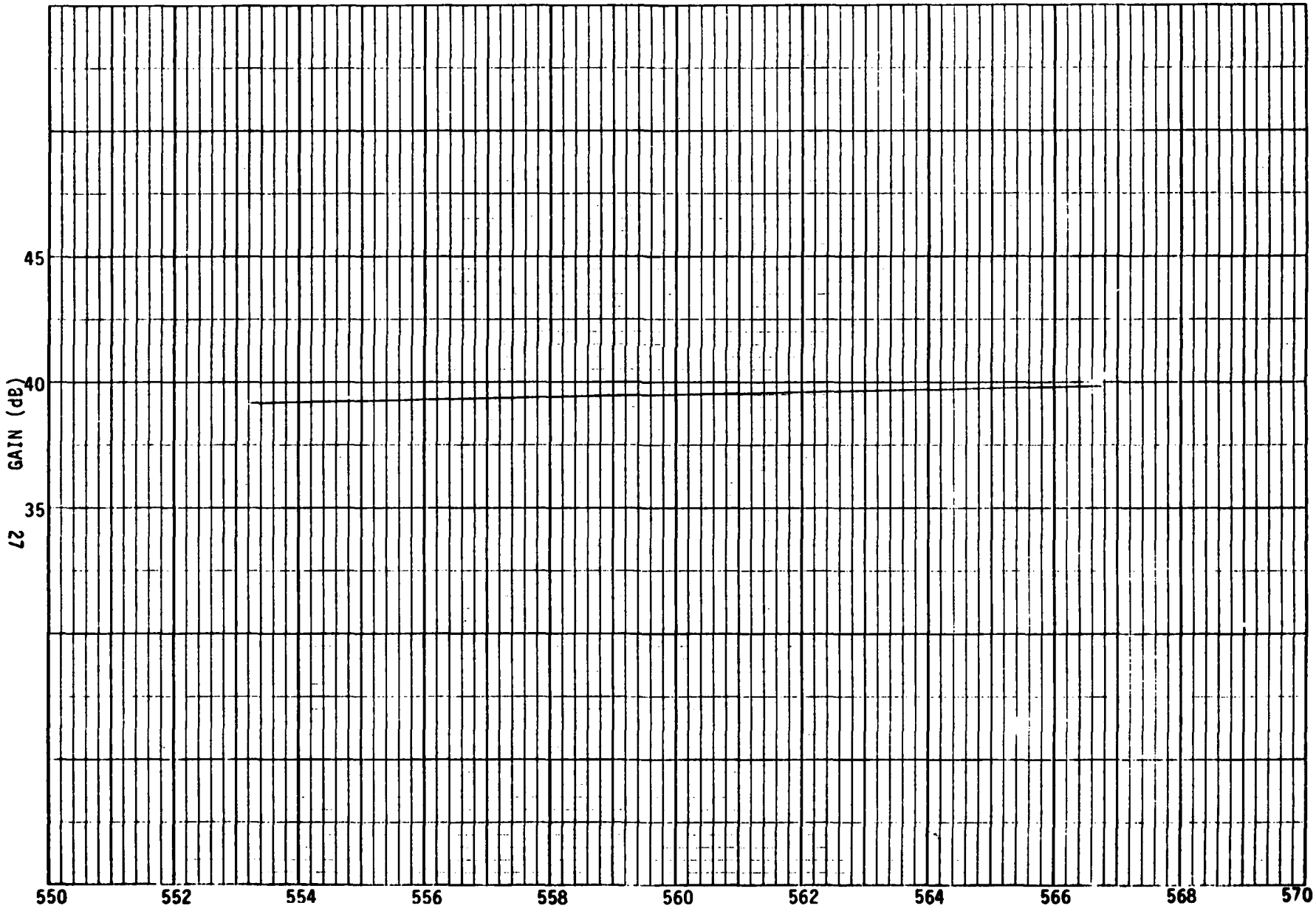
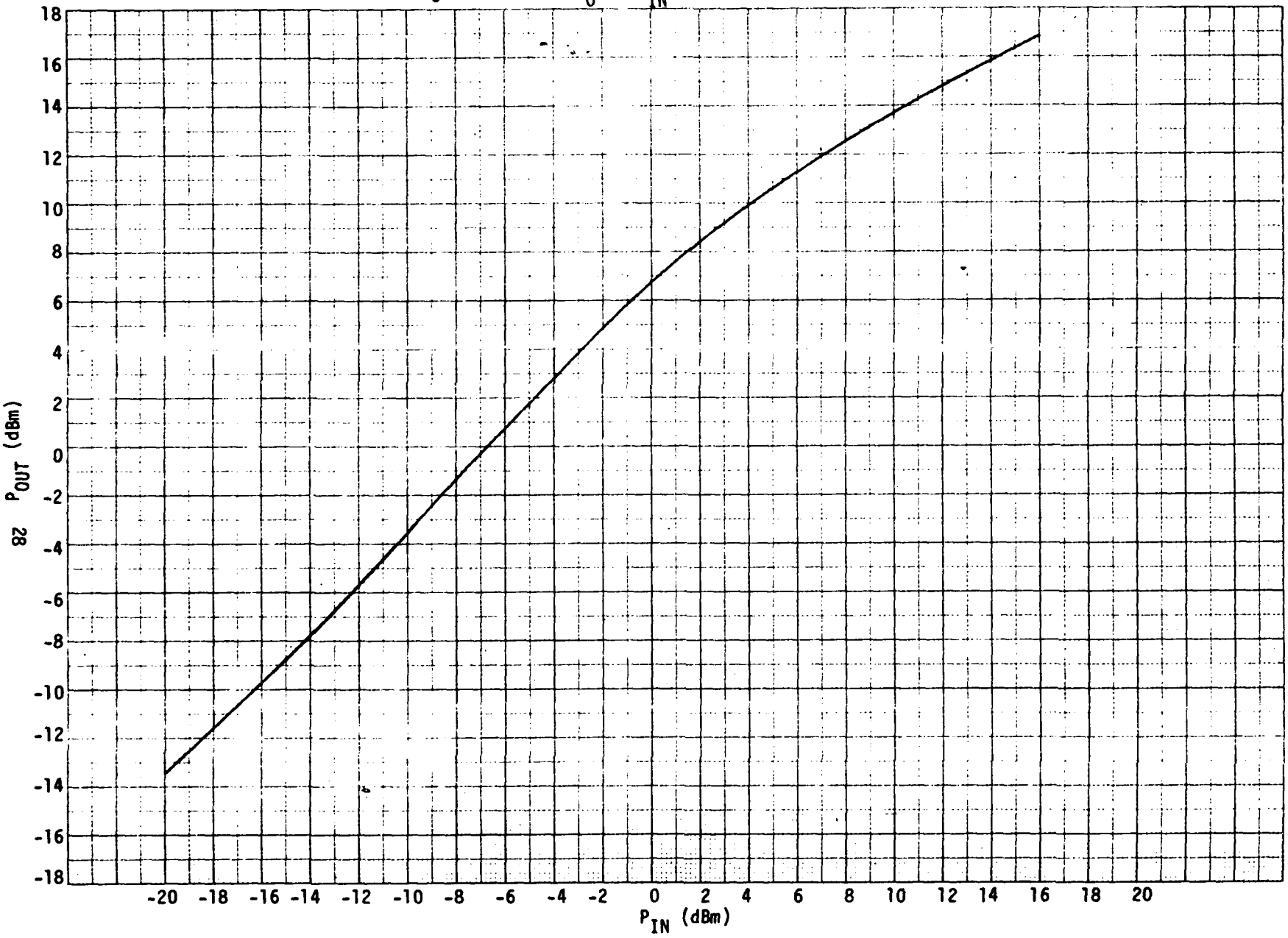


Figure 2-18. P_0 vs P_{IN}, FEEDBACK AMPLIFIER



NAME A SZURISMAN	TITLE MICROWAVE OSC. AMP CHAIN EFR 91 AMP #1	DWG. NO.
SMITH CHART FORM 82-BSPR(9-66)	KAY ELECTRIC COMPANY, PINE BROOK, N.J. © 1966. PRINTED IN U.S.A.	DATE 11/9/79

IMPEDANCE OR ADMITTANCE COORDINATES

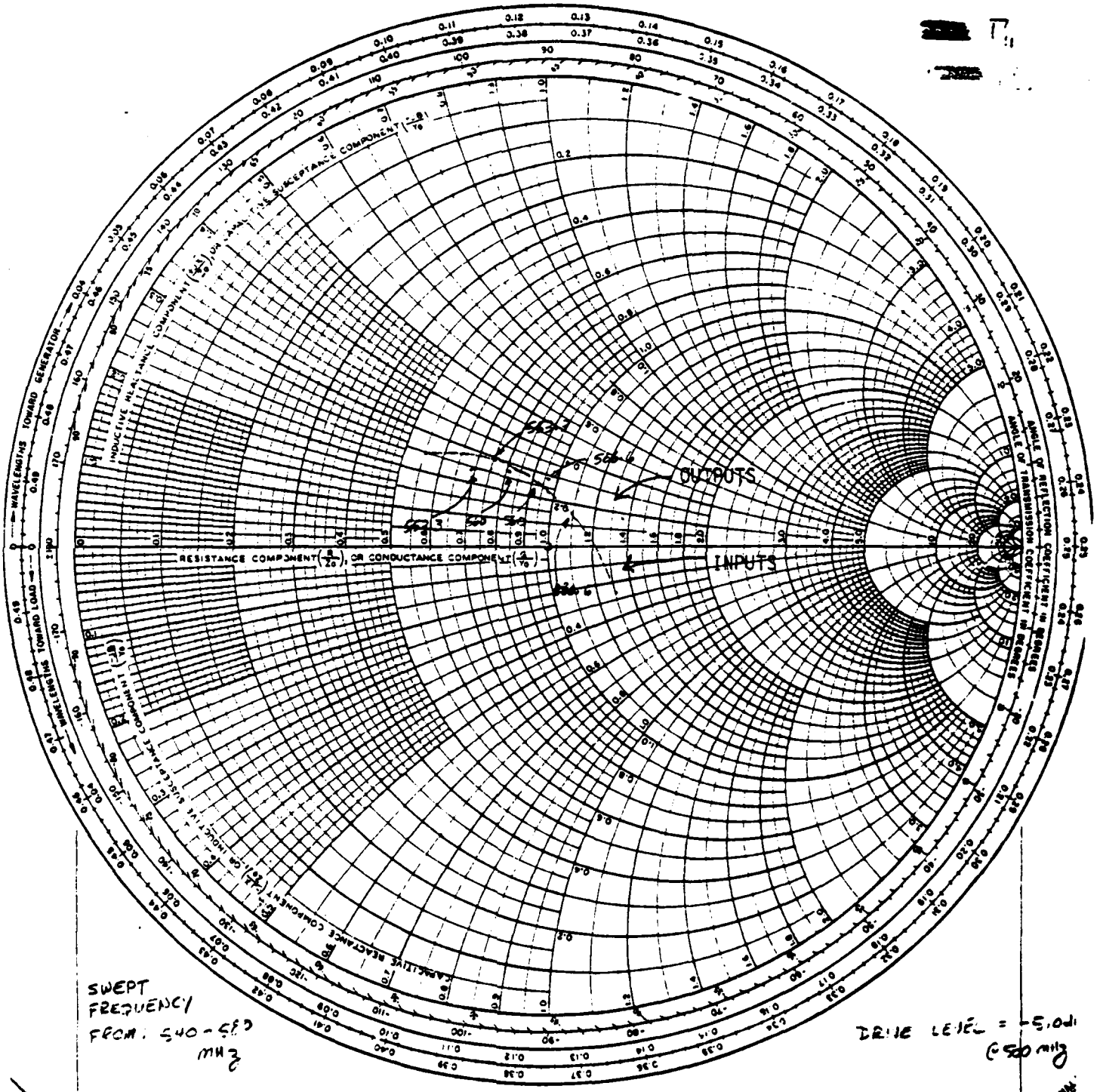
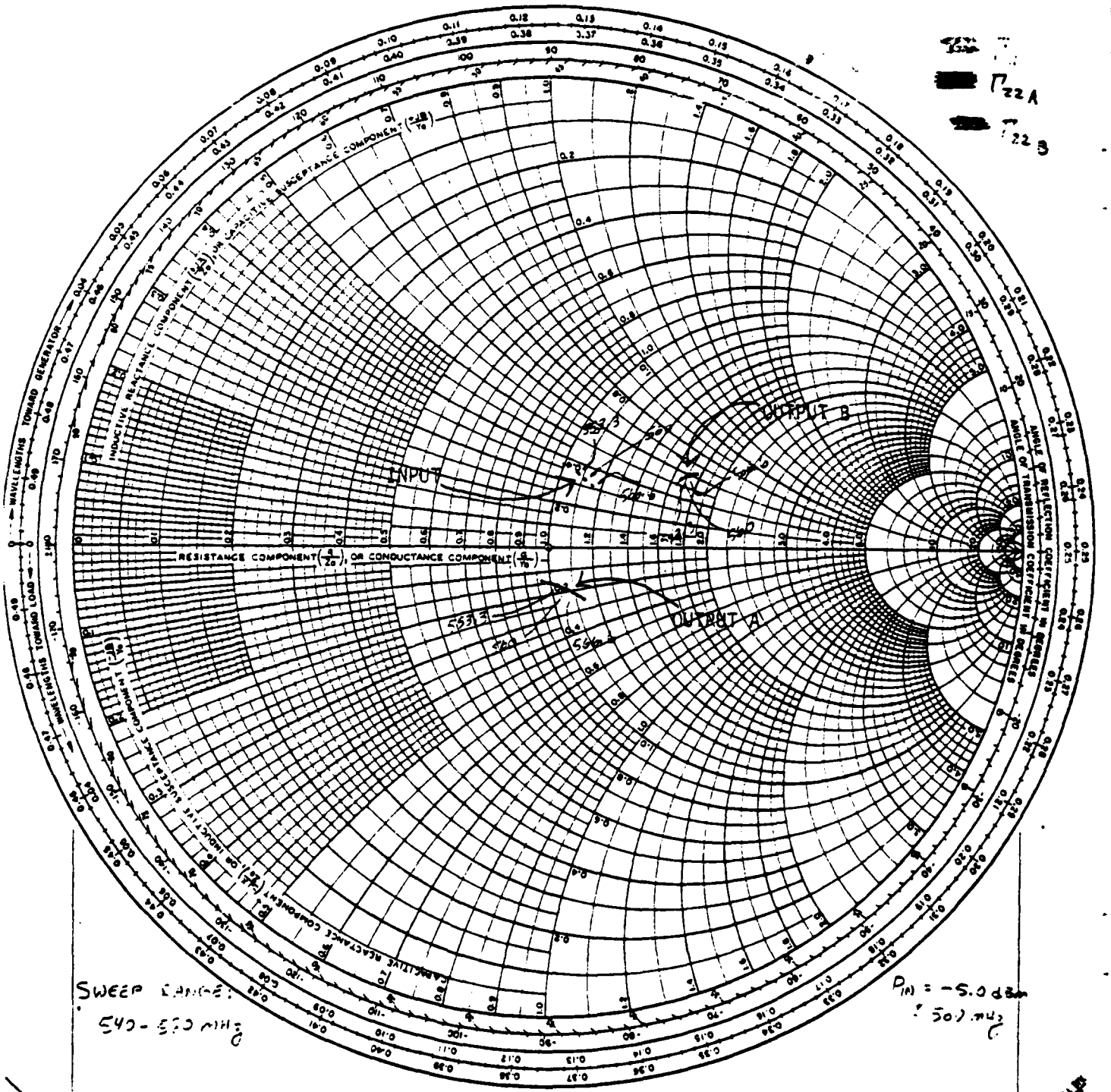


Figure 2-19. AMPLIFIER STAGES 1 AND 2

NAME M. SCANLAN	TITLE 10 OSC AMPLIFIER #3 EPE 96	DWG. NO.
SMITH CHART FORM 92-BSPR(9-66)	KAY ELECTRIC COMPANY, PINE BROOK, N.J. © 1966. PRINTED IN U.S.A.	DATE 11/7/79

IMPEDANCE OR ADMITTANCE COORDINATES



SWEEP RANGE: 540 - 560 MHz

$P_{IN} = -5.0$ dBm @ 50 MHz

Figure 2-20. AMPLFIER OUTPUT STAGE REFLECTION COEFFICIENTS

A MEDA-CHART

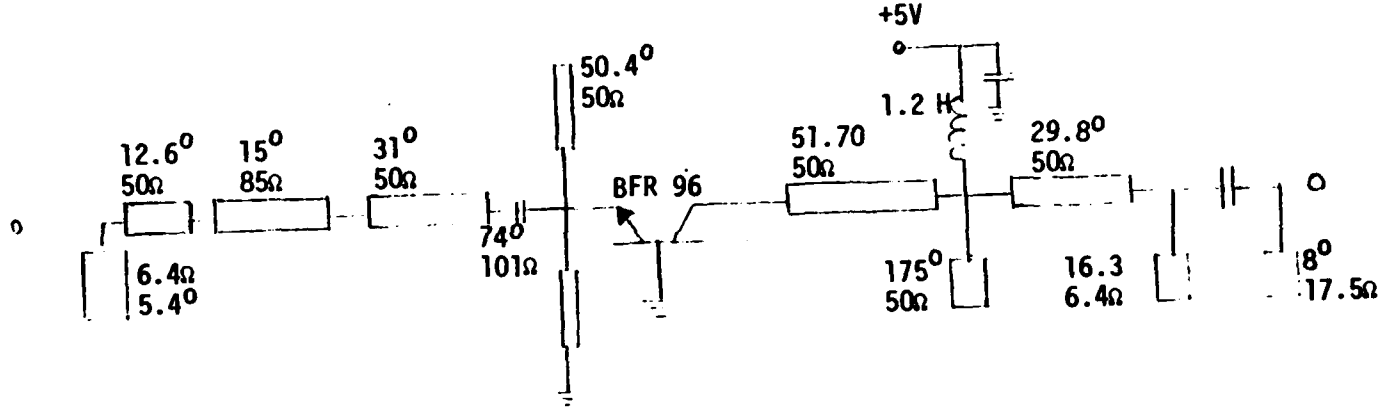


Figure 2-21. TRIPLER SCHEMATIC

Figure 2-22 is a plot of the power out versus power in for the tripler, and Figure 2-23 is tripler output power versus frequency at the 1680 MHz frequency.

(4) Output Amplification

Two basic methods exist to amplify the output of the tripler to the desired .5W level. These are by amplifying the tripler output in a power amplifier, or by injection locking a .5W oscillator to the tripler output. The amplifier approach, assumed to be a class C amplifier for power efficiency purposes, is very straight-forward. However, because of the frequency of operation and the power level desired, the necessary transistor is relatively expensive ($30-$50). The injection locked oscillator (ILO) can make use of very low-cost readily available devices, but suffers from the problem of holding lock over a relatively wide bandwidth, temperature range, and load impedances.

Power Amplifier

The schematic for the power amplifier is shown in Figure 2-24 . Because of the desired gain and frequency of operation, the TRW 54601 was selected and biased to operate in a class C condition. The amplifier's measured response is shown in Figure 2-25 . We note that it provides a minimum of 525 mW at 1700 MHz, increasing up to 661 mW at 1660 MHz.

ILO

Injection locking tests were performed on both the existing radiosonde oscillators (VIZ Industries design, 200 mW output), and a second oscillator design developed by TRW for this program. The original oscillator design,

Figure 2-22. P_{OUT} vs P_{IN} FOR TRIPLER

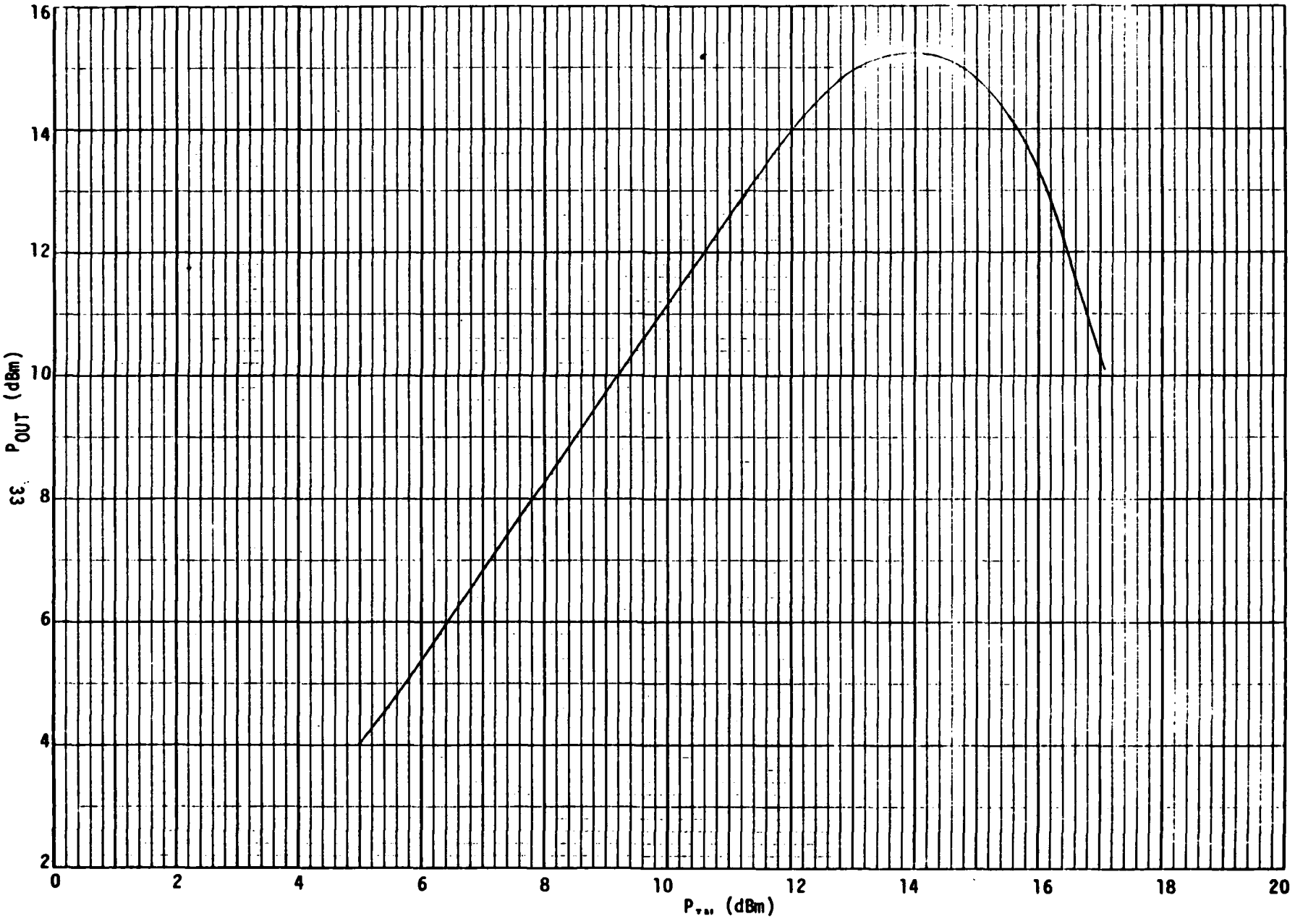
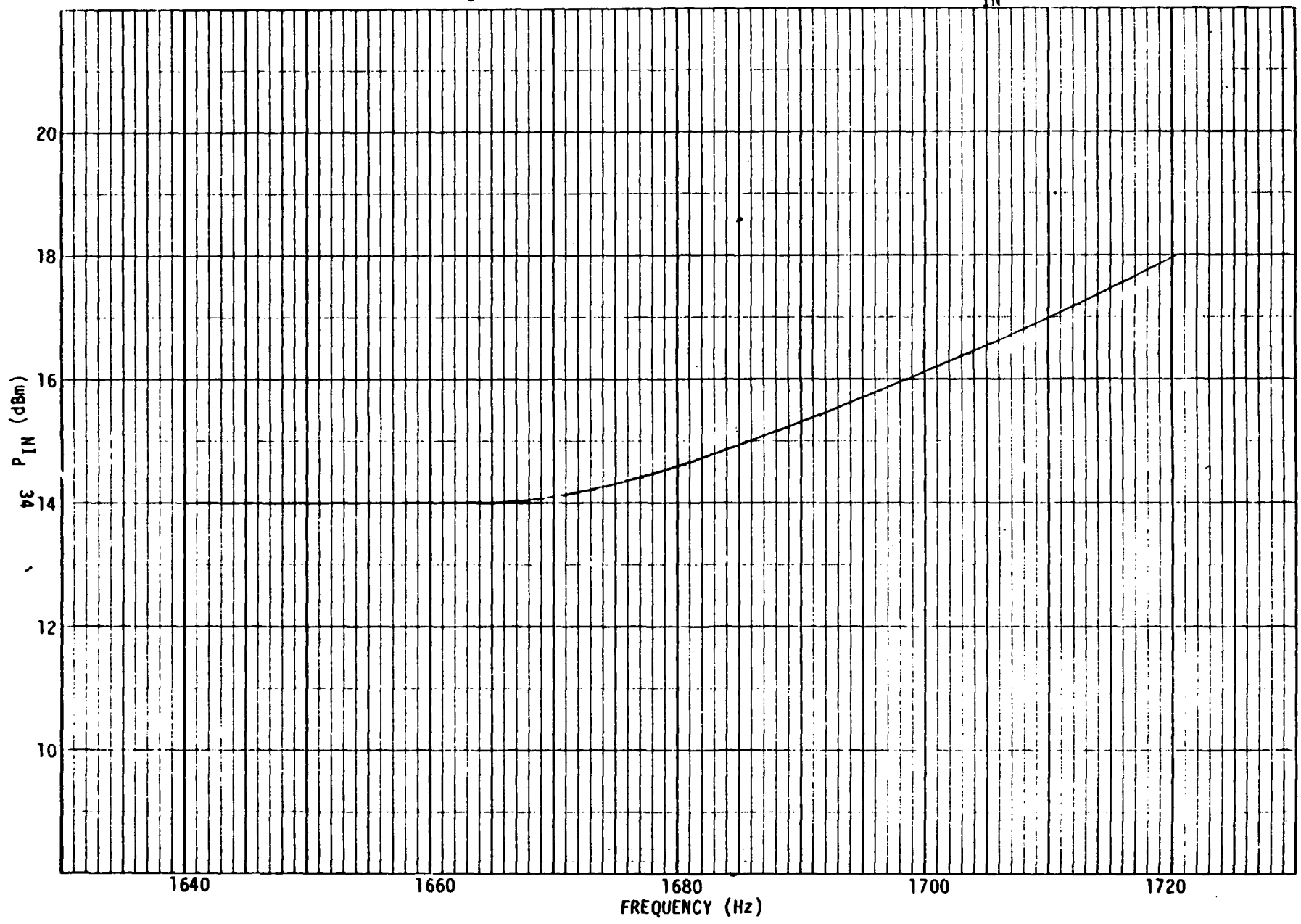


Figure 2-23. TRIPLER OUTPUT POWER vs FREQUENCY (P_{IN} = +15 dBm)



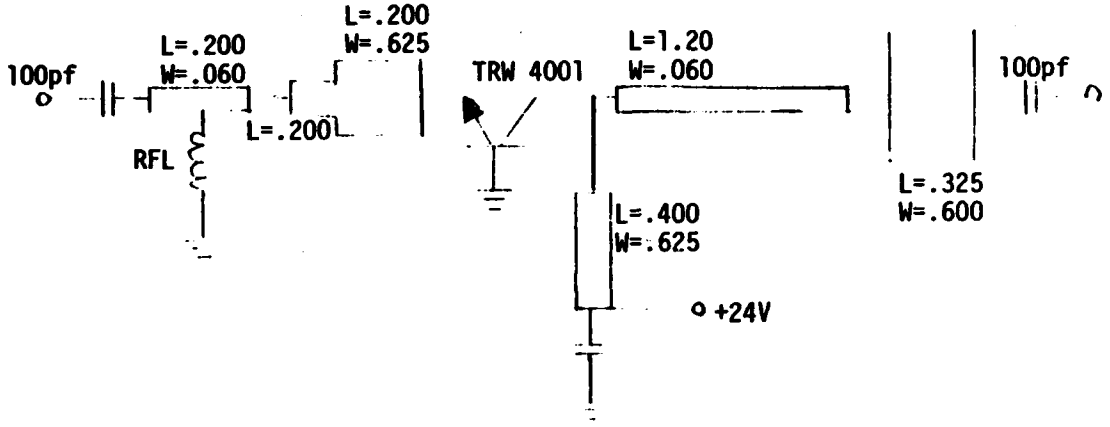
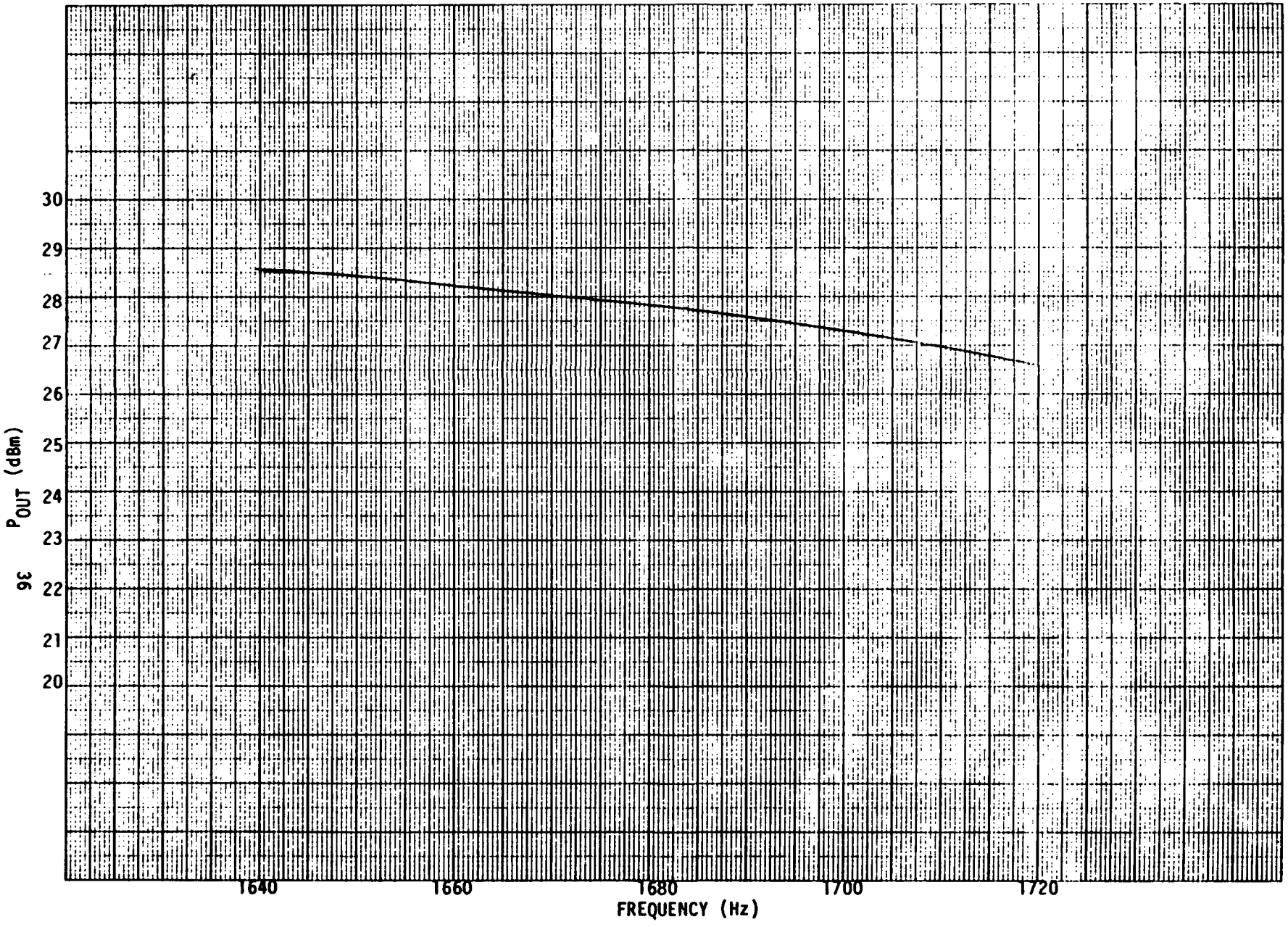


Figure 2-24. POWER AMP SCHEMATIC

Figure 2-25. OUTPUT POWER vs FREQUENCY, POWER AMPLIFIER



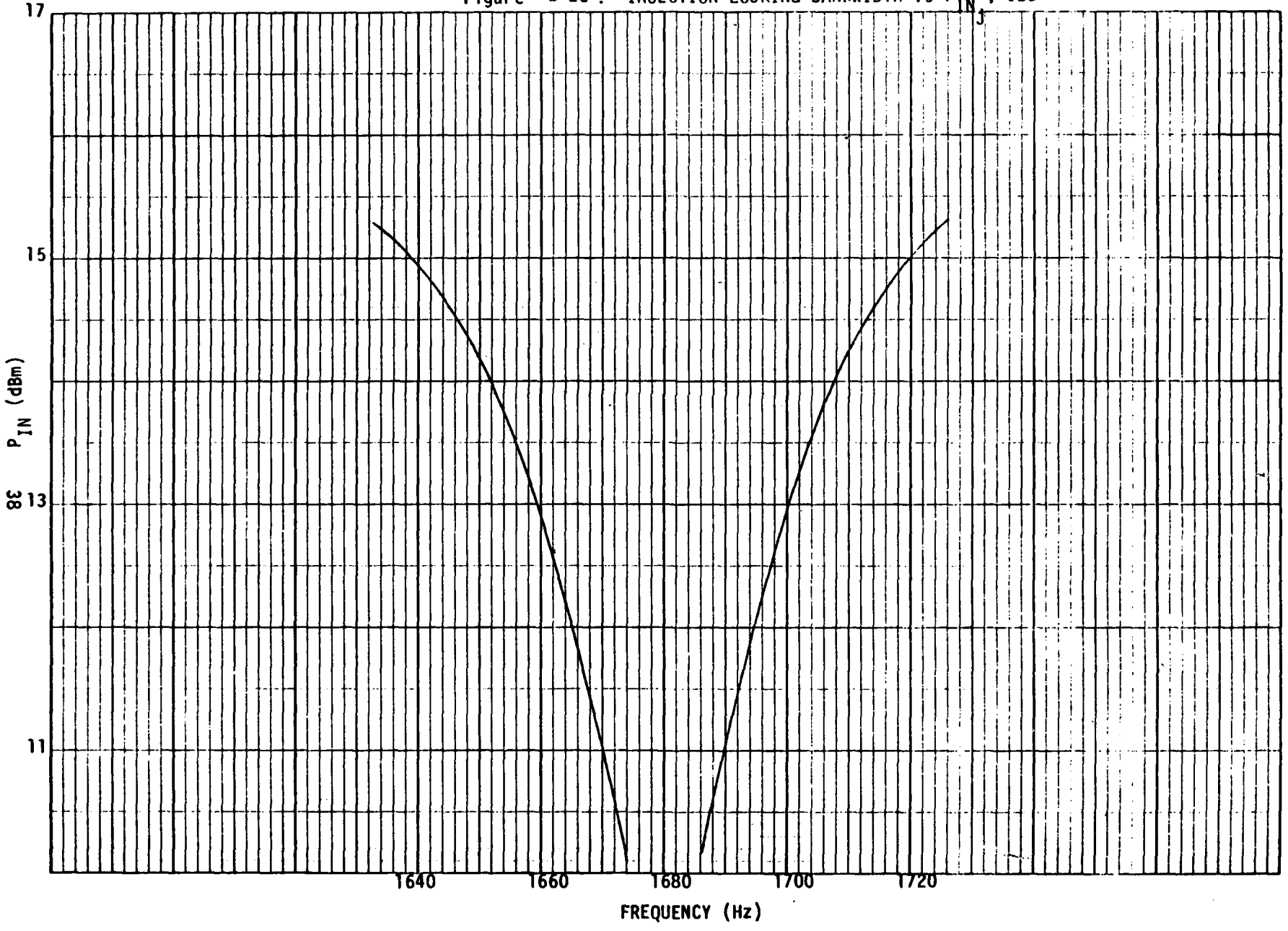
described in the previous semi-annual report, exhibited unreliable locking characteristics and was therefore discarded. Figure 2-26 shows the injection locking characteristics of the TRW oscillator with the injection locking signal at the fundamental. It is seen that the TRW design with a fundamental injection lock signal at about +17 dBm provides over 80 MHz of locking bandwidth, which is considered adequate over the desired temperature and load characteristics in which this oscillator must operate.

The schematic of the TRW injection locked oscillator is shown in Figure 2-27. Note that a pecularity of this oscillator is that the output is the most optimum locking point. This is contrary to intuition and makes the output sensitive to load VSWRs. This is an area of design which must be further studied during the advanced development phase.

c. Oscillator package

Figure 2-28 is a sketch of the package and Figure 2-29 is a photograph of one of the actual deliverable breadboard oscillators. These units contain two PC boards housed inside the 3" x 5" x 1.75" metal container. For breadboard purposes, any of the four SAW filters may be selected by lifting the cover off the box and resoldering the jumper wire at the input and output of the SAW filter. For the advanced development models, a technique such as plugging the desired filter into the correct socked is envisioned. Again, this area should be further developed in the next phase of the program. Figure 2-30 shows a photograph of the top board containing the SAW oscillator. Figures 2-31 and 2-32 show the top and bottom sides of the second board containing the power amplifier and control circuitry and the X3 circuit, respectively.

Figure 2-26. INJECTION LOCKING BANDWIDTH vs P_{IN_J}, ILO



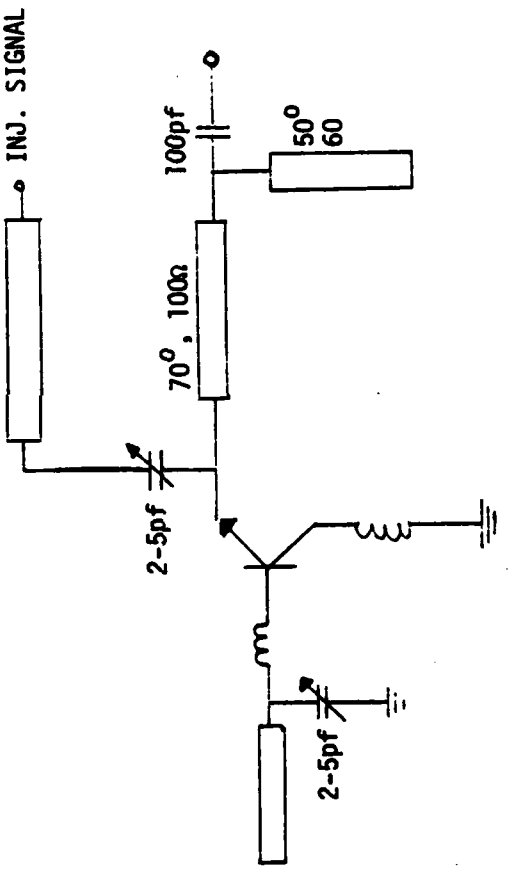


Figure 2-27. ILO SCHEMATIC

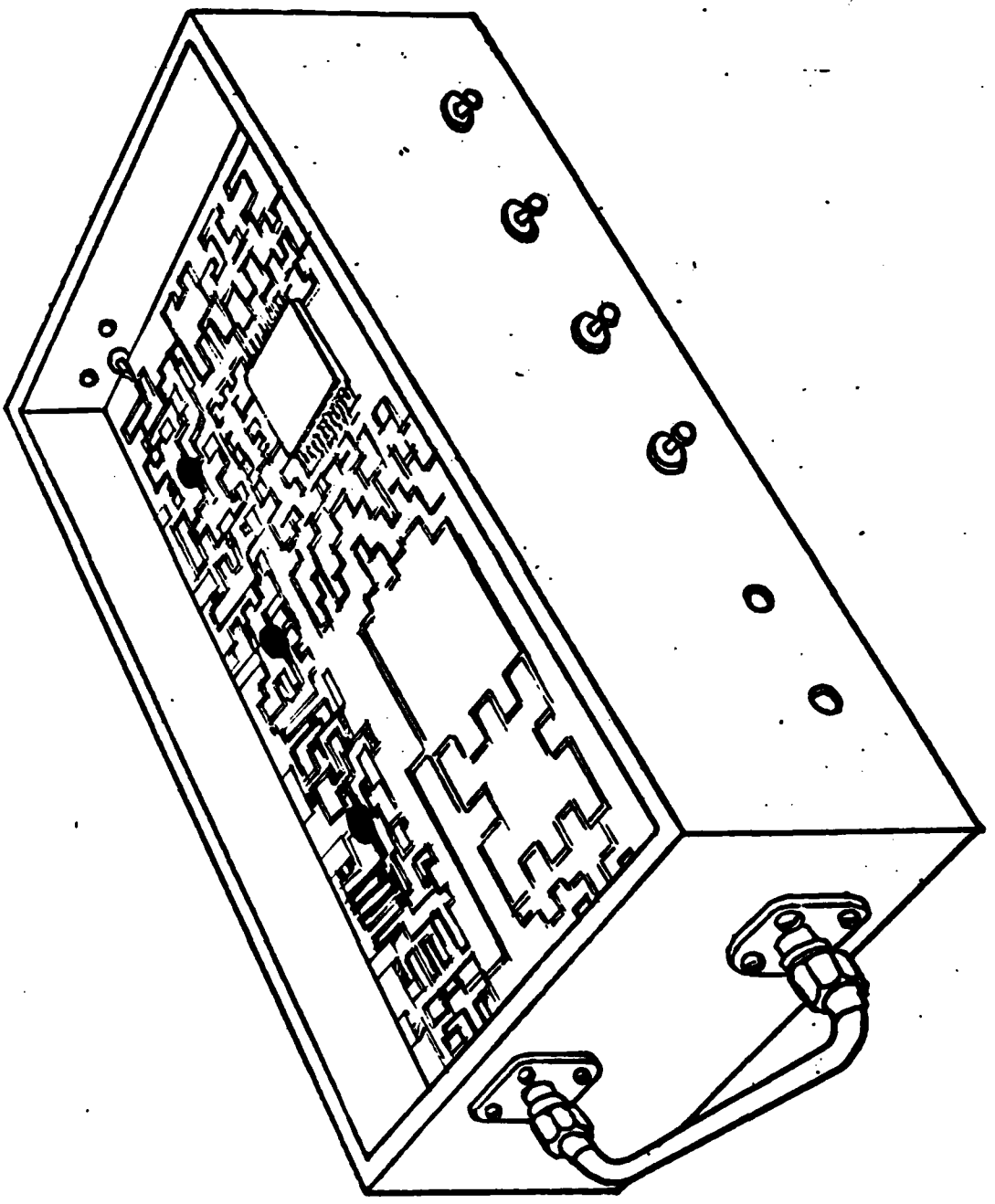


Figure 2-28. Oscillator Housing

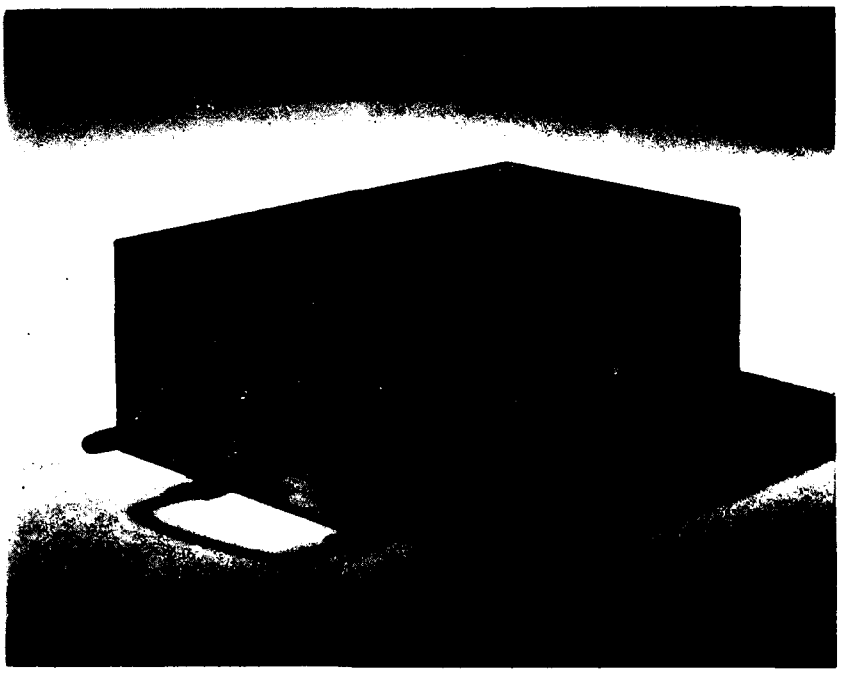


Figure 2-29. PHOTOGRAPH OF PACKAGED MICROWAVE OSCILLATOR

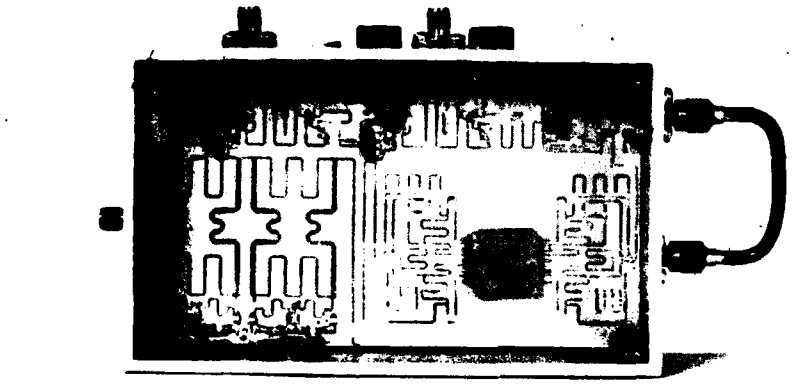


Figure 2-30. SAW OSCILLATOR BOARD

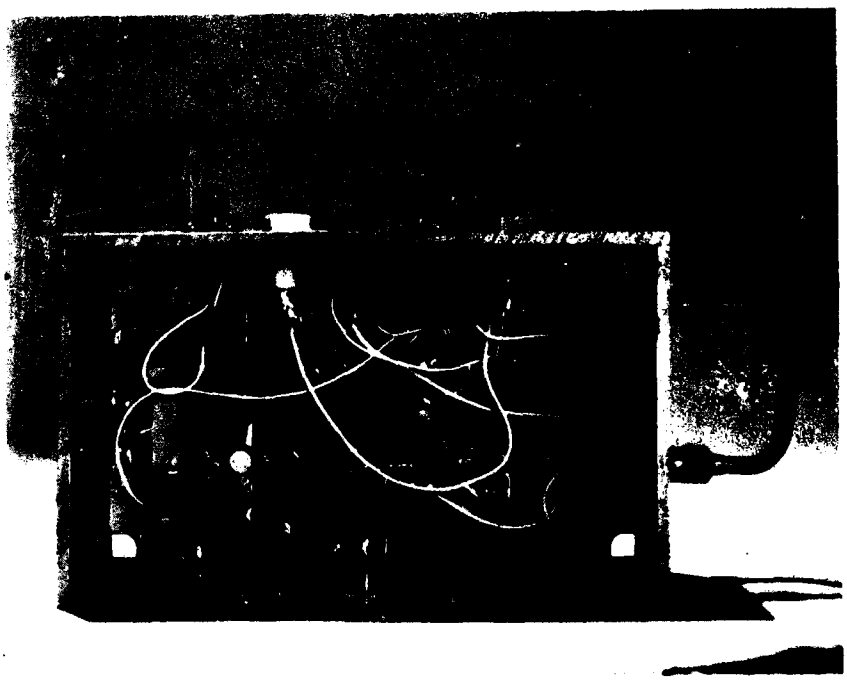


Figure 2-31. POWER AMPLIFIER AND CONTROL CIRCUITRY BOARD

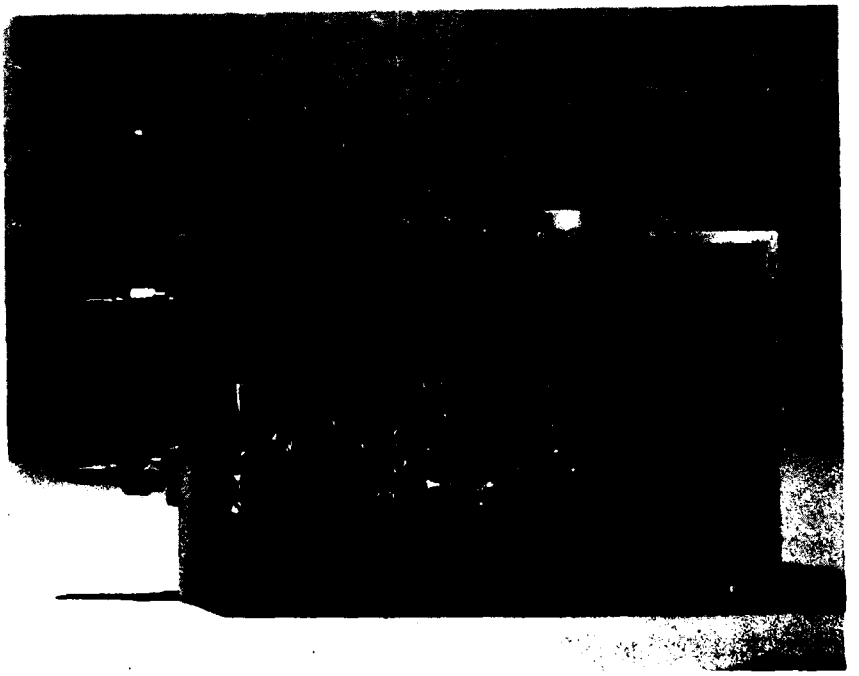


Figure 2-32. X3 CIRCUIT

d. Oscillator Results

Completed oscillator test data compiled in this section for evaluation of unit performance was measured on both deliverable prototype oscillators. The compiled data consists of the following individual test categories:

- o P_{OUT} vs Frequency (Tuning Range)
- o Settability (Frequency Settability)
- o Temperature Stability
- o Spurious Levels
- o Frequency Pulling (Loading Effects)
- o DC Power Consumption
- o AM-FM

In the data that follows, each of the above seven measurements can be found in sequence, progressing from prototype breadboard No. 1, Channels 1-4, to prototype breadboard No. 2, Channels 1-4.

The test methods employed in compiling the representative oscillator test data are as follows:

1) P_{OUT} vs Frequency

Adjustment of phase shifter tuning voltage over full in-band range, measurement of output power, and fundamental frequency. (+25°C ambient temperature, nominal line voltages.)

2) Settability

After a one-minute power-off condition, measurement of the output fundamental frequency as a function of increasing time following turn-on. Drift of oscillator due to initial thermal and electrical transients. (+25°C ambient temperature, nominal line voltages.)

3) Temperature Stability

Upon setting the oscillator output signal midway in one of each of the four SAW bands, the drift of the carrier frequency is monitored over the temperature range of -70°C to +70°C. (2.0 MHz frequency span resolution, nominal line voltages.)

4) Spurious Levels

Signal spectrum of output carrier is viewed from DC to 5.0 GHz. Spurious signals present due to SAW oscillator and oscillator output components were noted. (+25°C ambient temperature, nominal line voltages.)

5) Frequency Pulling

The effect of an oscillator load consisting of a 6 dB pad placed at the end of a variable phase shifter is viewed through a directional coupler as the load is varied through 360° of phase. The corresponding carrier frequency variation is noted by a spectrum analyzer. (+25°C ambient temperature, nominal line voltages.)

6) DC Power Consumption

The input line voltage levels of the oscillator are varied from nominal (+24V and +13V), to maximum (+26.4V and +14.3V), and minimum (+21.6V and +11.7V). The corresponding nominal, maximum and minimum line currents are measured. (+25°C ambient temperature.)

7) AM-FM

Measurement of 0-100% amplitude modulation signal levels at fundamental output frequency. (Fundamental signal output on/off isolation upon application of AM signal input.)

Verification of 10-100 KHz FM signal bandwidth around carrier fundamental. (+25°C ambient temperature, nominal line voltages.)

Figure 2-33. OUTPUT POWER vs FREQUENCY, BREADBOARD NO. 1, CHANNEL NO. 1

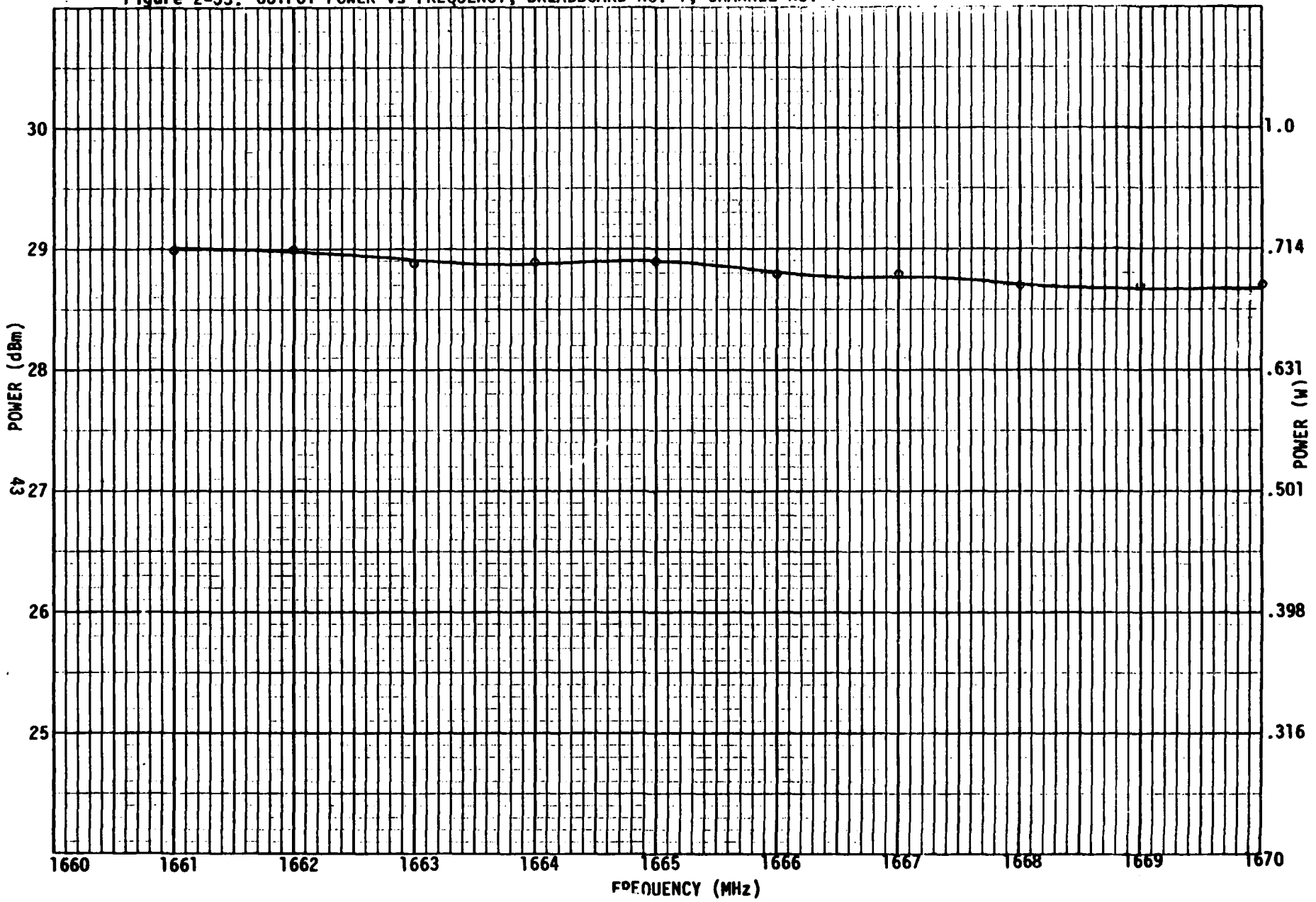


Figure 2-34. SETTABILITY, BREADBOARD NO. 1, CHANNEL NO. 1

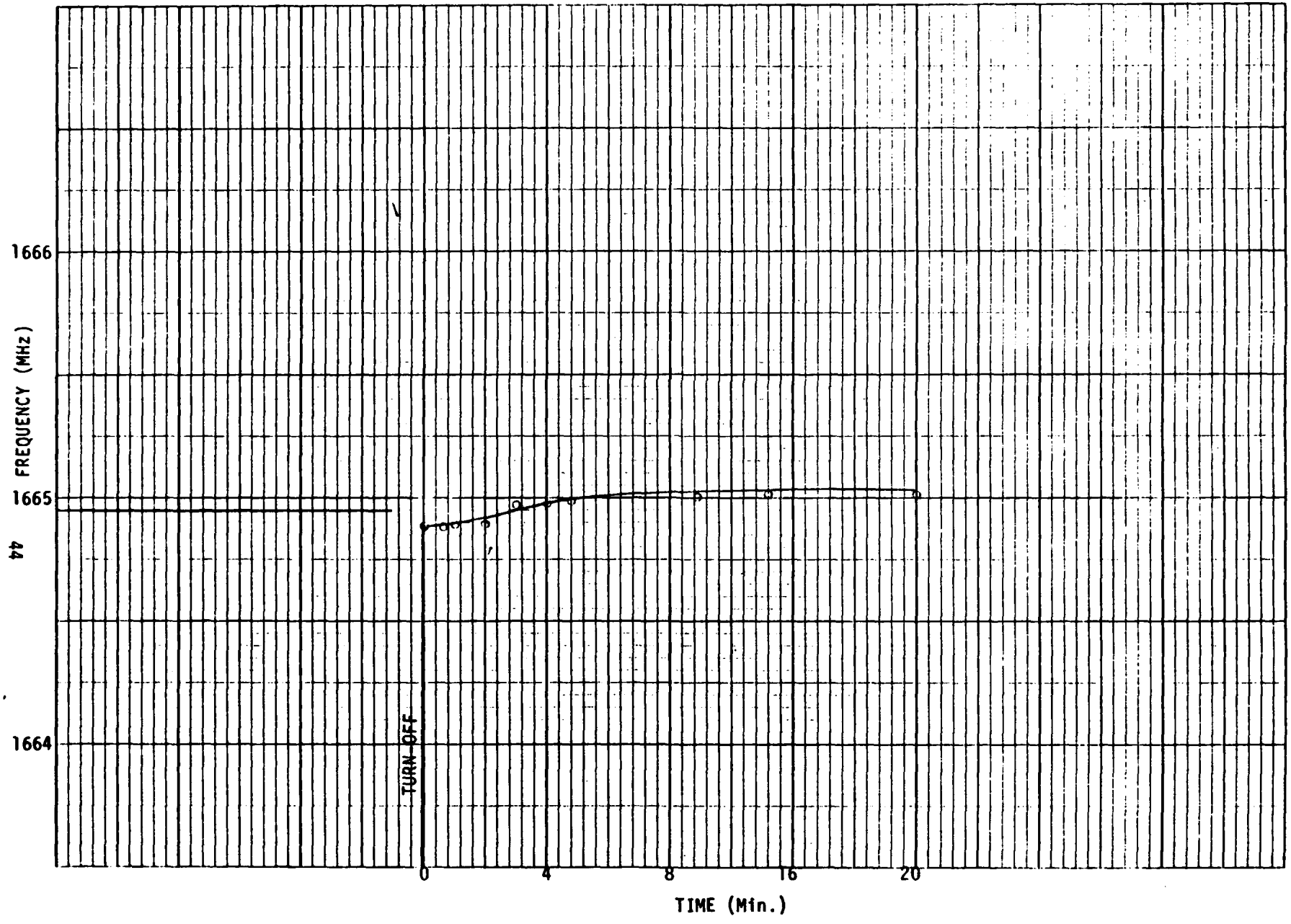


Figure 2-35. TEMPERATURE TEST, BREADBOARD NO. 1, CHANNEL NO. 1

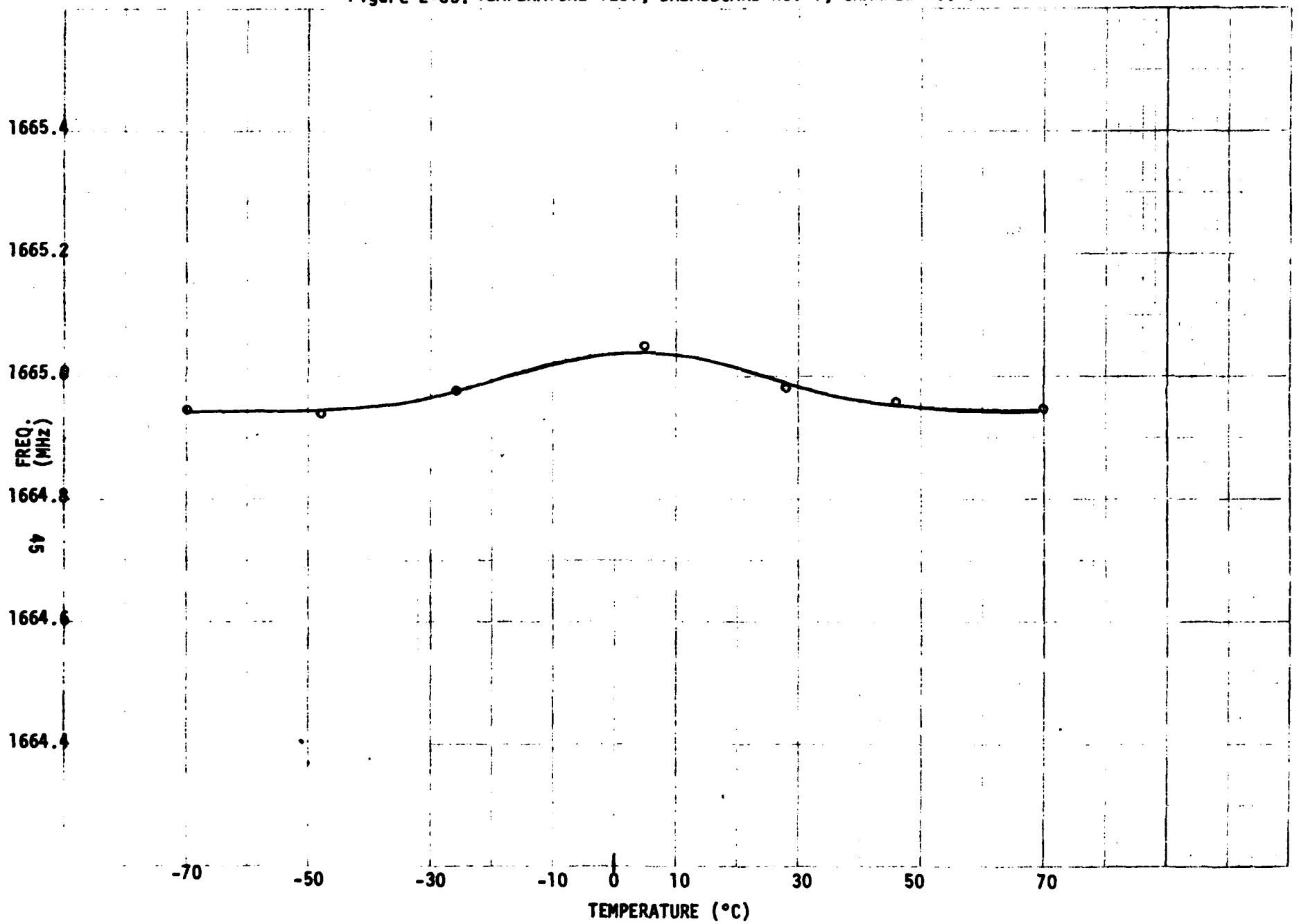


Table 2-2. PERFORMANCE

BREADBOARD #1 CHANNEL #1

A) SPURIOUS LEVEL

FREQUENCY (MHZ)	ORIGIN	P_{OUT} (DBM)	P_{OUT} (DBM)
555.0	SAW FREQUENCY	-25.5	54.5
1110	2X SAW FREQ	-25.5	54.5
3330	2X F_{OUT}	+9.5	19.5
5071	3X F_{OUT}	-28.0	57.0

B) FREQUENCY PULLING

ΔF = 286 KHz ($\pm$143 MHZ)

C) BIAS

V	$I_{(MA)}$	$P_{(W)}$
13	166.0	2.16
24	98.3	2.36
11.7	139.9	1.64
21.6	82.5	1.78
14.3	166.5	2.38
26.4	114.1	3.00

D) AM (V_{IN} = 1.414V)

P_{ON} = +28.9 dBm

P_{OFF} = -10.0 dBm

Figure 2-36. OUTPUT POWER vs FREQUENCY, BREADBOARD NO. 1, CHANNEL NO. 2

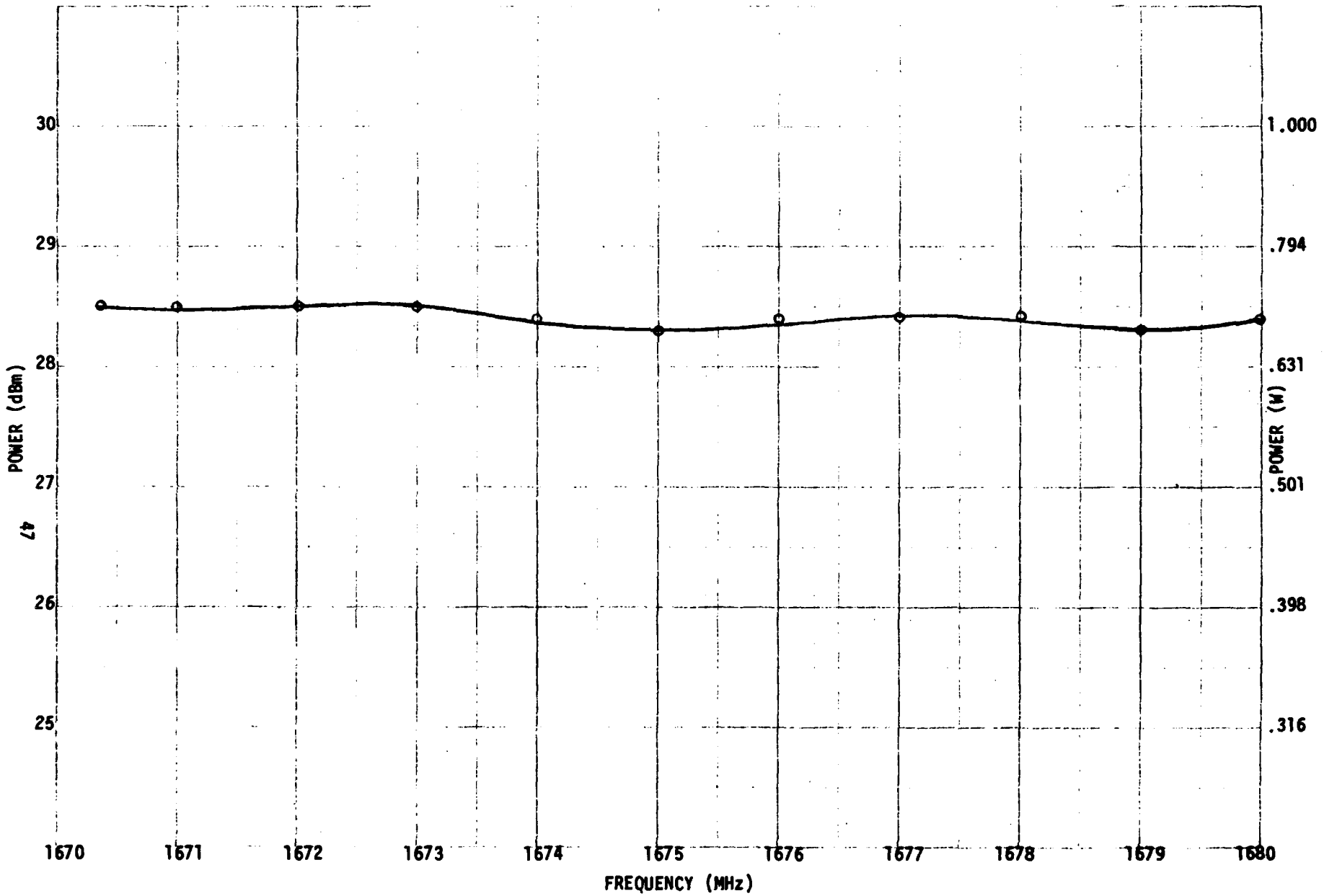


Figure 2-37. SETTABILITY, BREADBOARD NO. 1, CHANNEL NO. 2

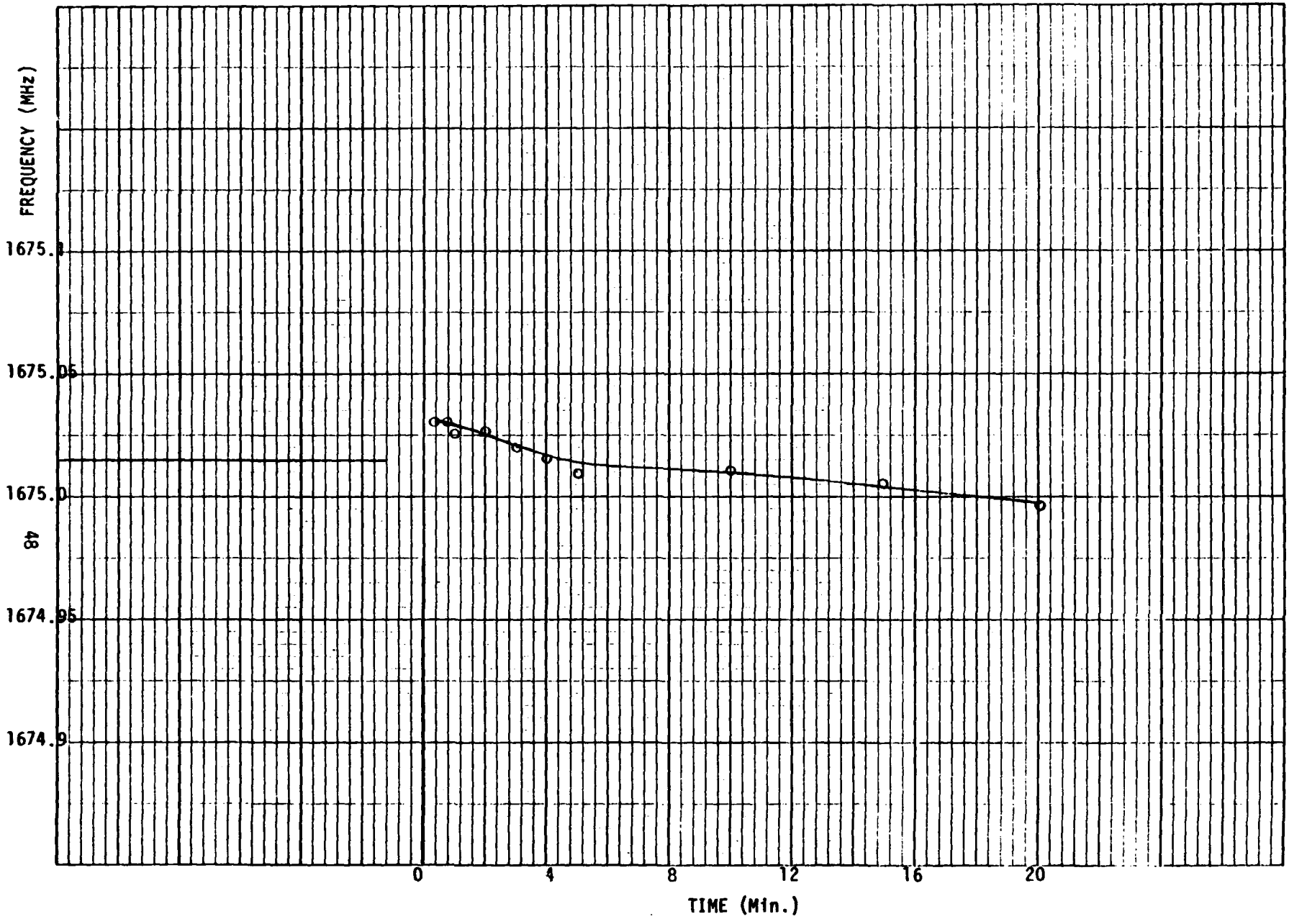


Figure 2-38. FREQUENCY vs TEMPERATURE, BREADBOARD NO. 1, CHANNEL NO. 2

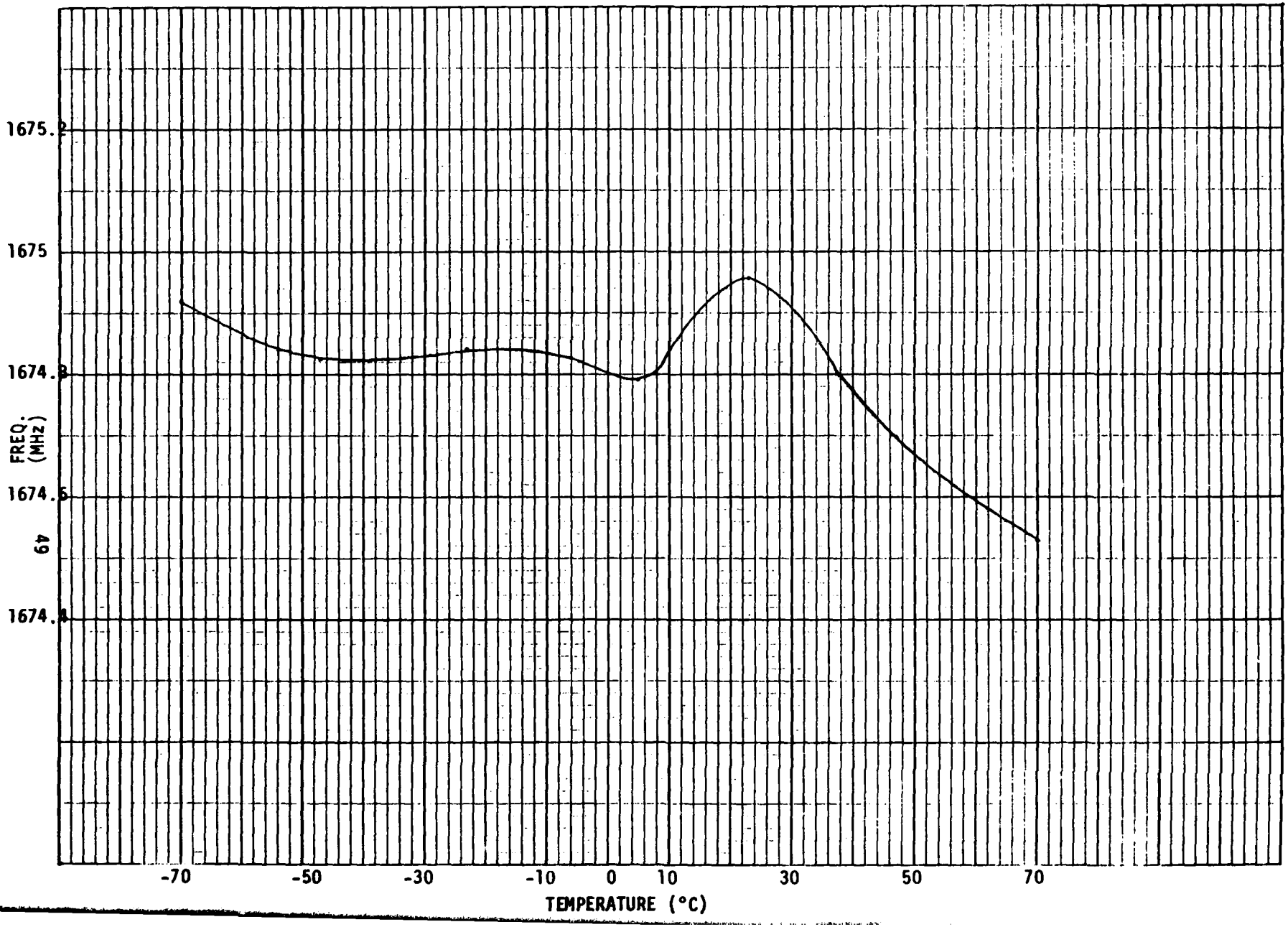


Figure 2-39. OUTPUT POWER vs FREQUENCY, BREADBOARD NO. 1, CHANNEL NO. 3

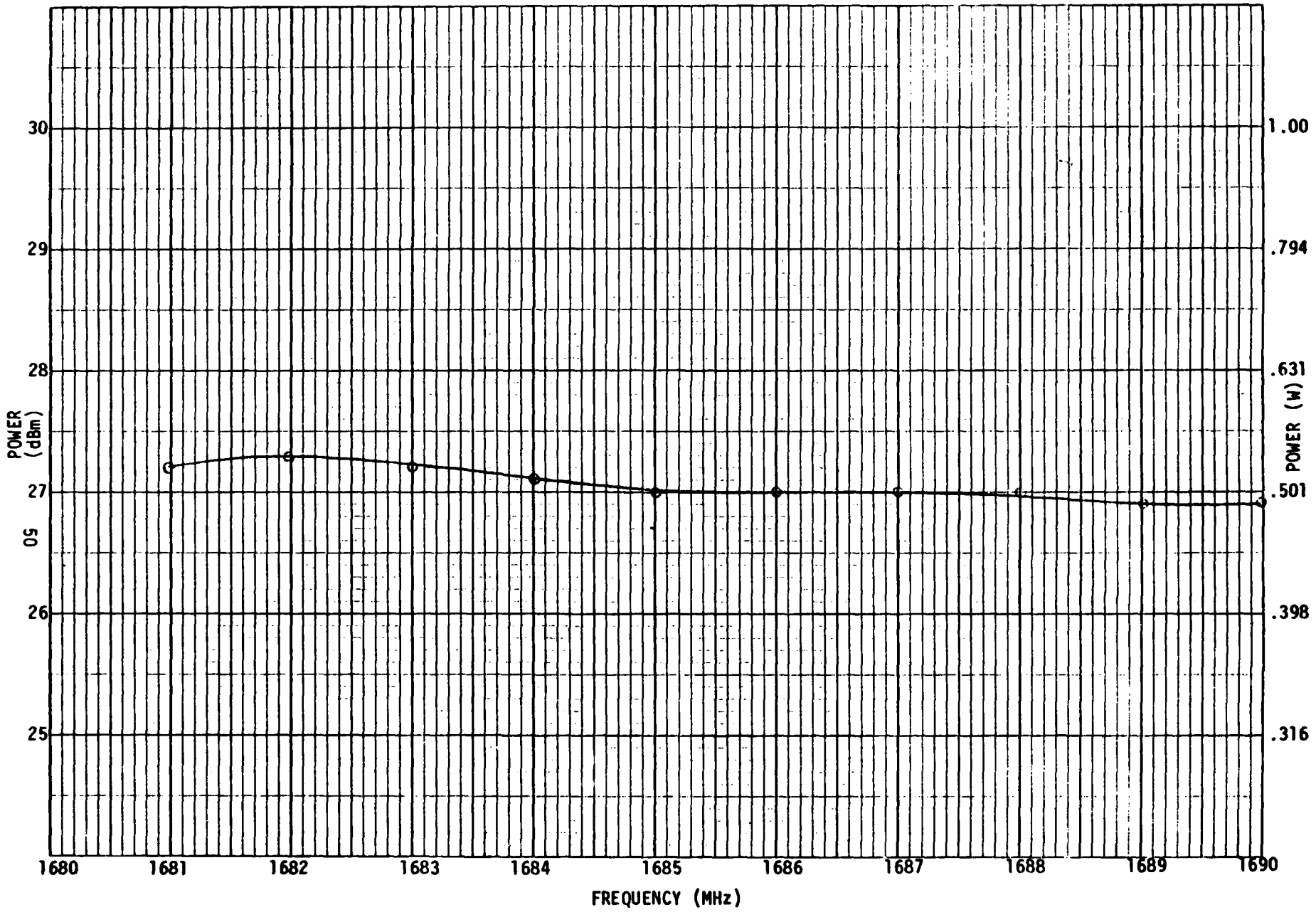


Figure 2-40. SETTABILITY, BREADBOARD NO. 1, CHANNEL NO. 3

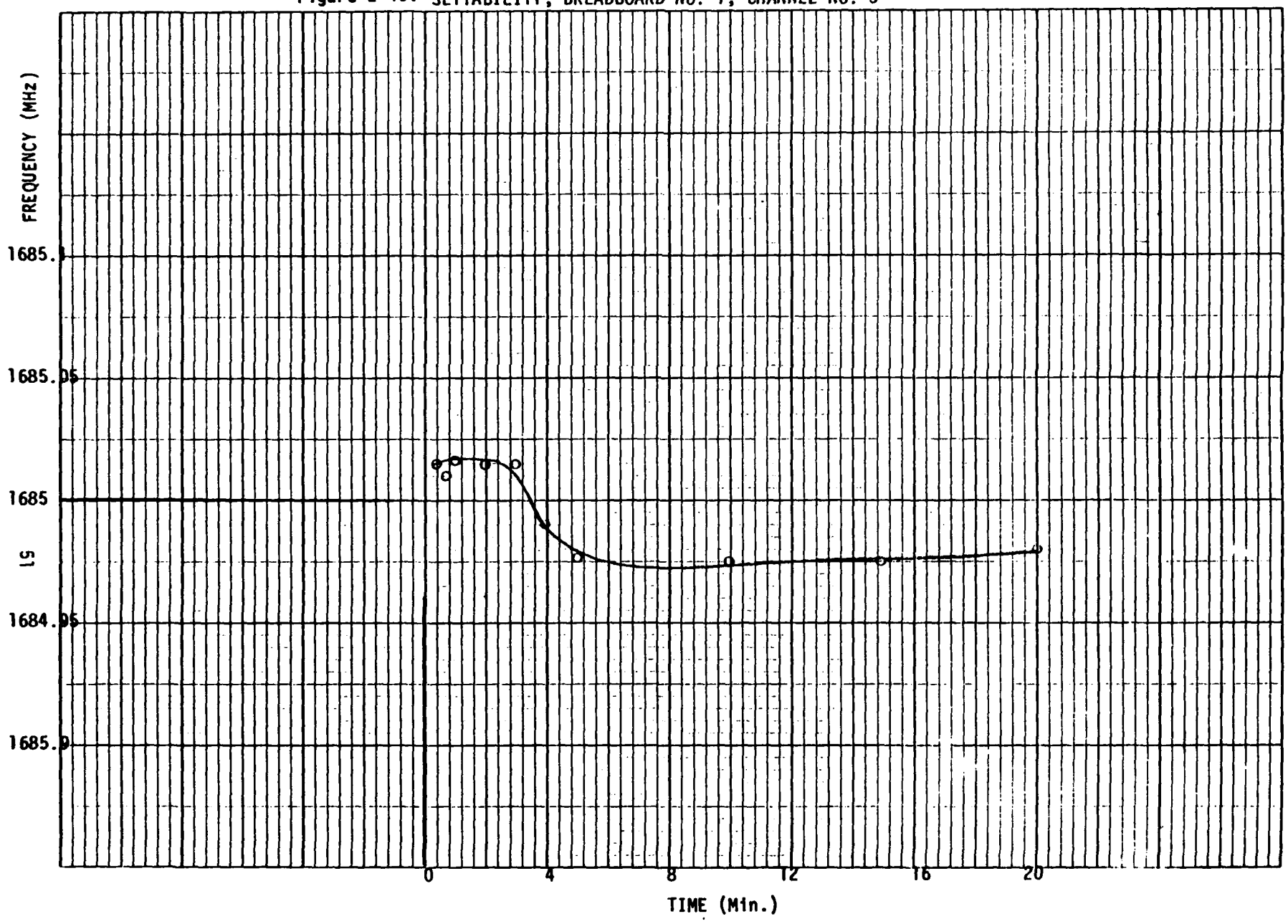


Figure 2-41. FREQUENCY vs TEMPERATURE, BREADBOARD NO. 1, CHANNEL NO. 3

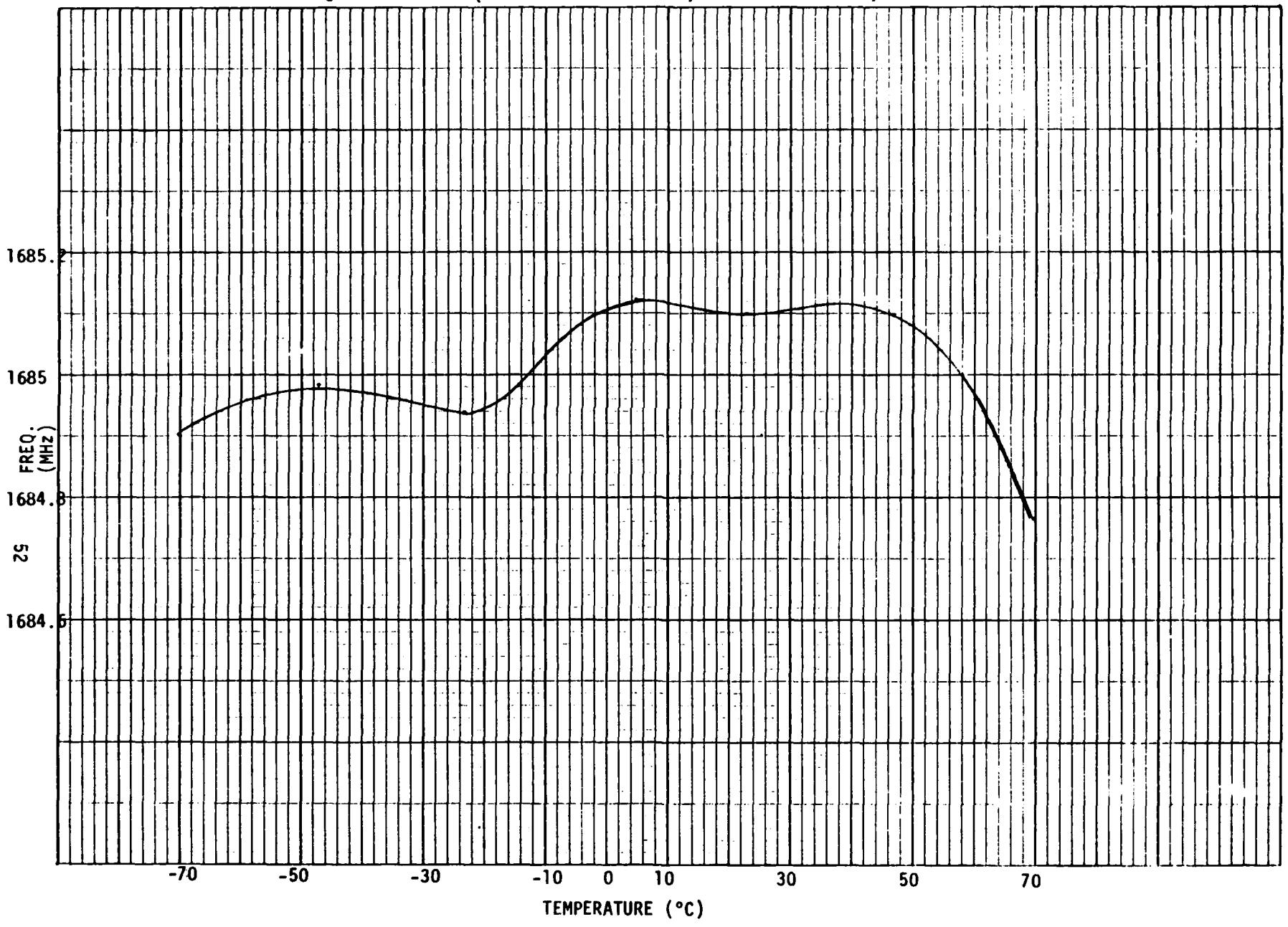


Figure 2-42. OUTPUT POWER vs FREQUENCY, BREADBOARD NO. 1, CHANNEL NO. 4

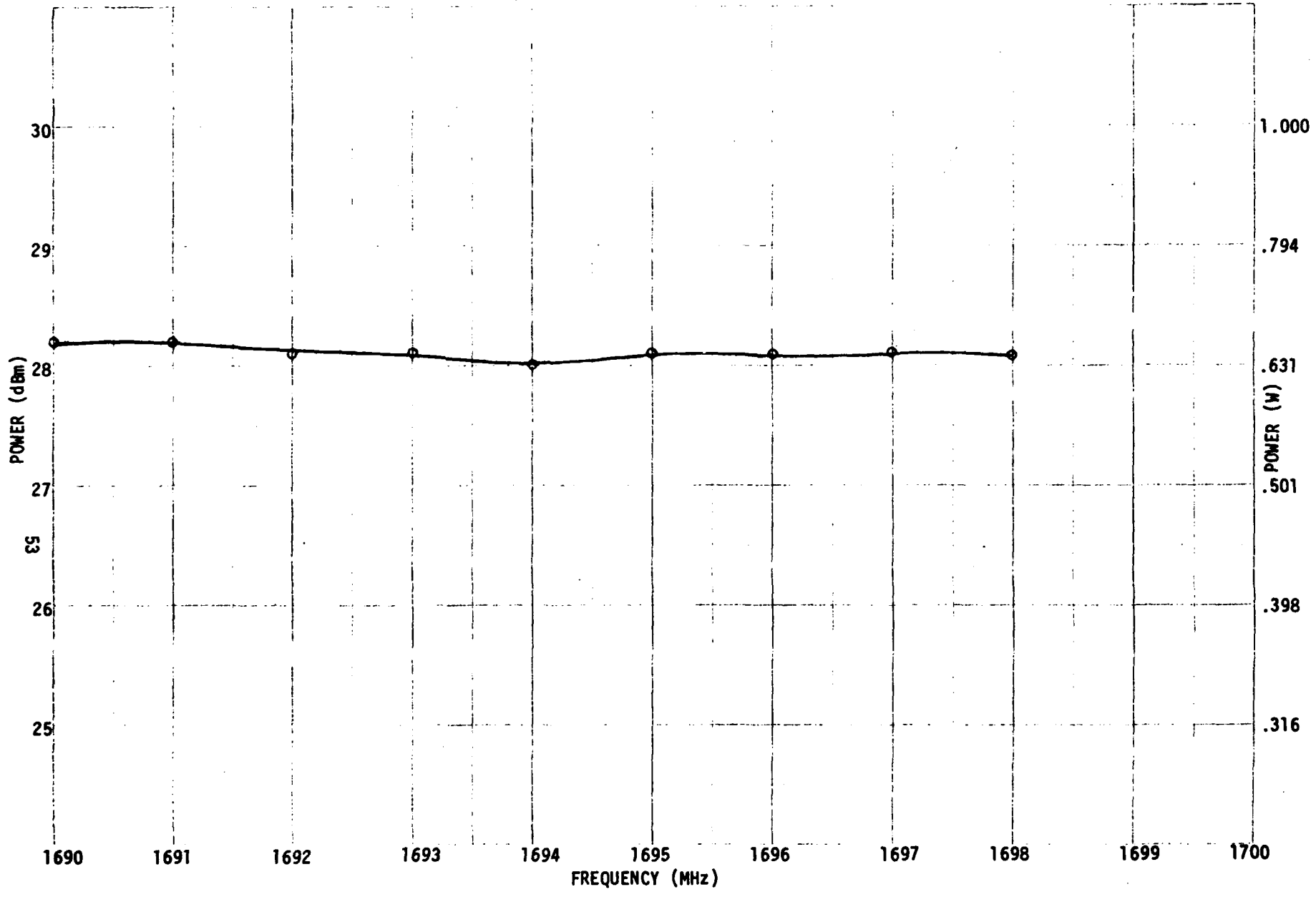


Figure 2-43. SETTABILITY, BREADBOARD NO. 1, CHANNEL NO. 4

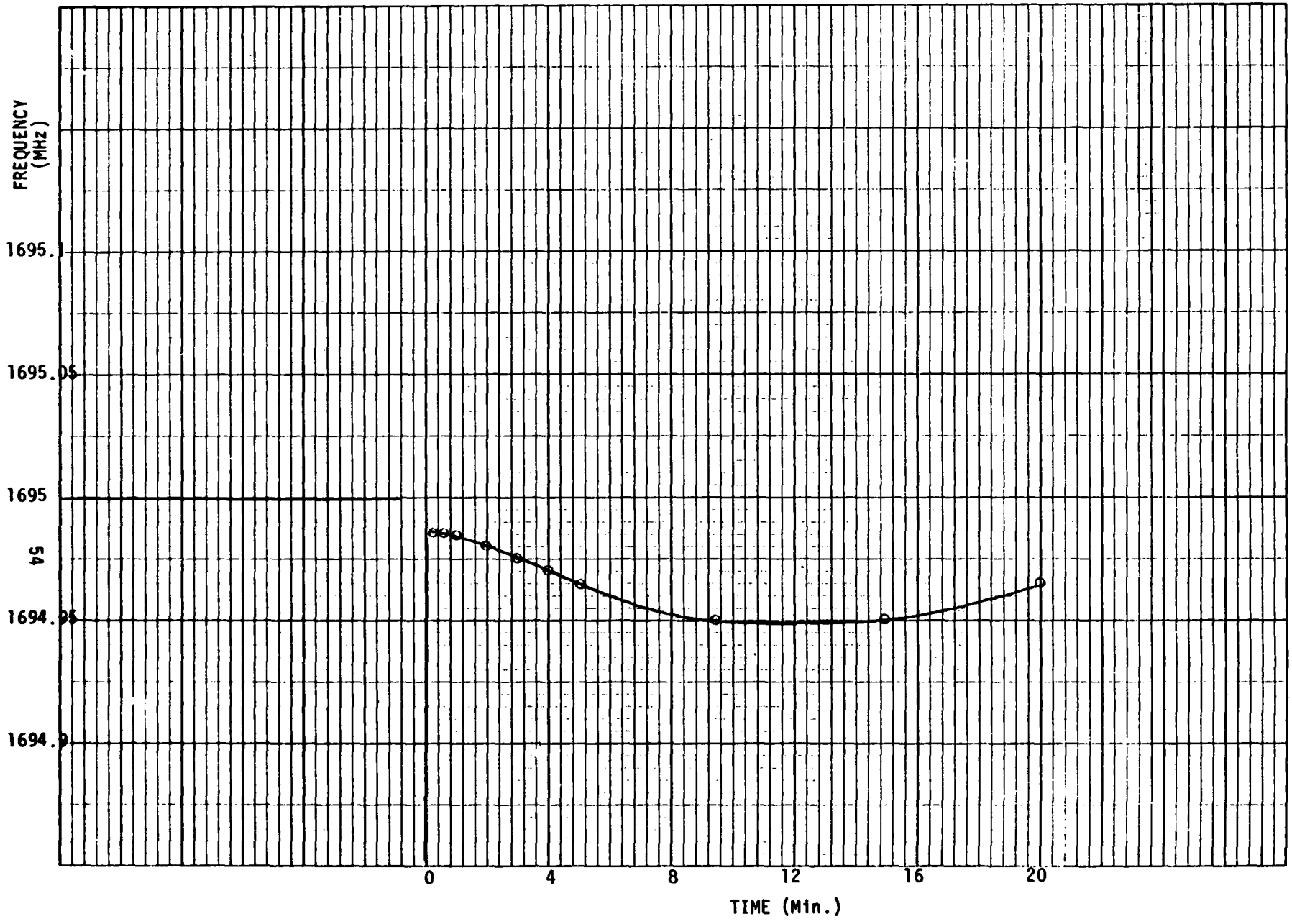


Figure 2-44. FREQUENCY vs TEMPERATURE, BREADBOARD NO. 1, CHANNEL NO. 4

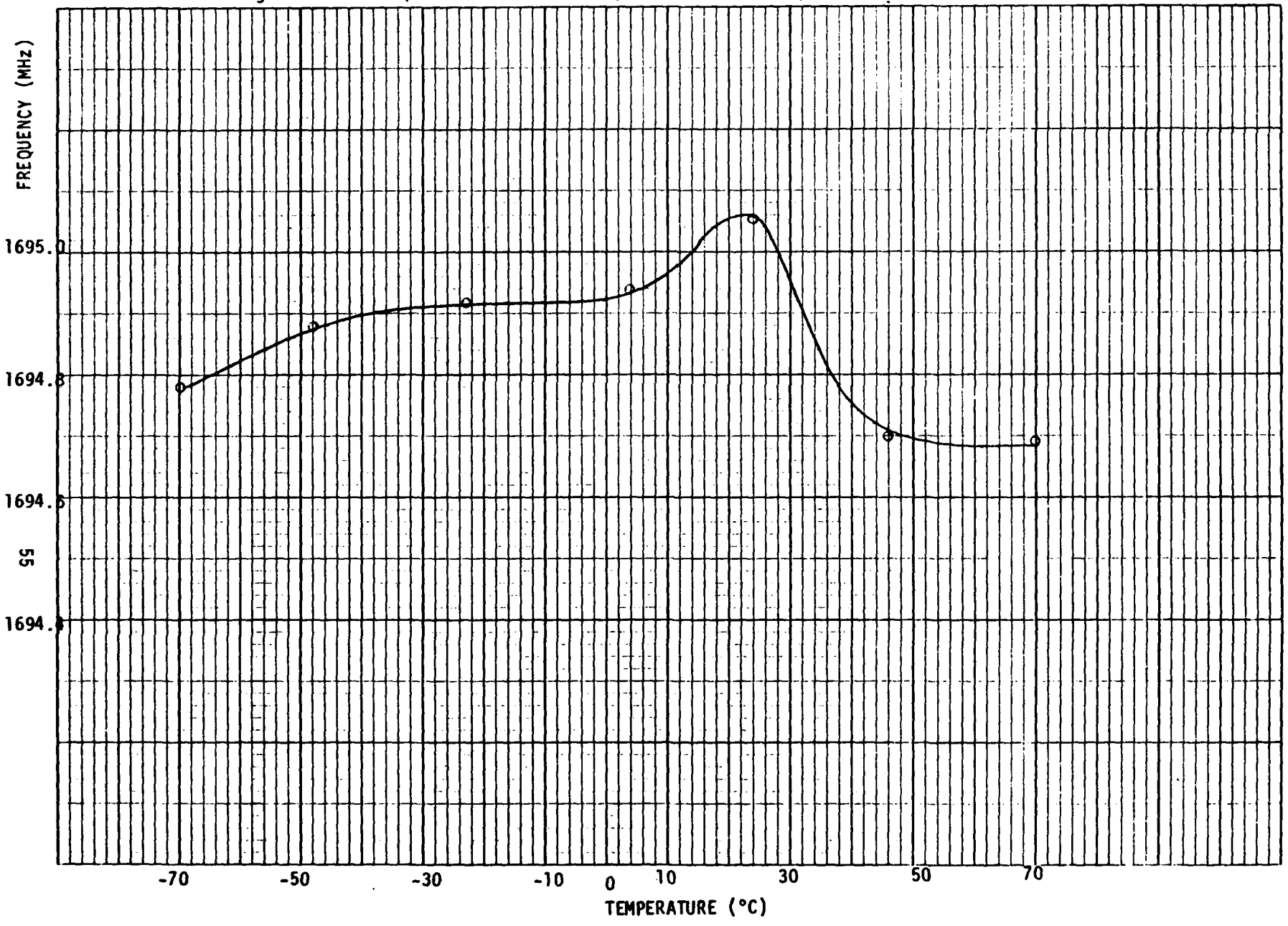


Table 2-3. TEMPERATURE STABILITY OF BREADBOARD OSCILLATOR NO. 1

BREADBOARD OSCILLATOR #1	CHANNEL #	TEMP °C	FREQ MHZ	POUT (DBM)	f (PPM)
	1	+70	1664.662	+28.60	242
		+ 5	1665.066	+28.40	
		-70	1664.950	+28.10	
	2	+70	1674.527	+28.40	257
		+23	1674.957	+28.60	
		-70	1674.921	+28.60	
	3	+70	1684.764	+28.20	214
		+ 5	1685.124	+28.10	
		-70	1684.904	+28.00	
	4	+70	1694.687	+27.80	222
		+23	1695.061	+28.10	
		-70	1695.785	+28.00	

Figure 2-45. OUTPUT POWER VS FREQUENCY BREADBOARD #2 CHANNEL #1

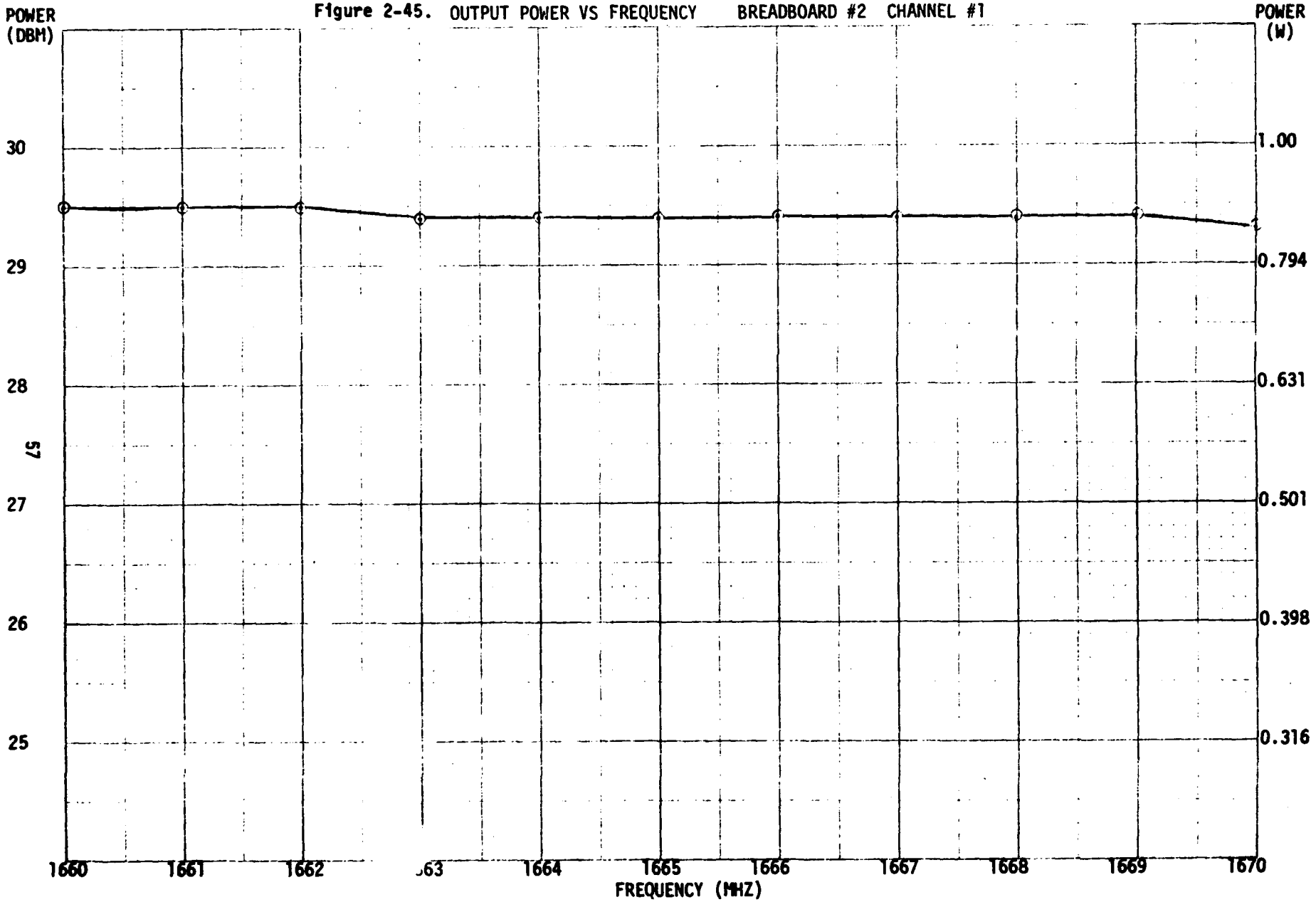


Figure 2-46. SETABILITY BREADBOARD #2 CHANNEL #1

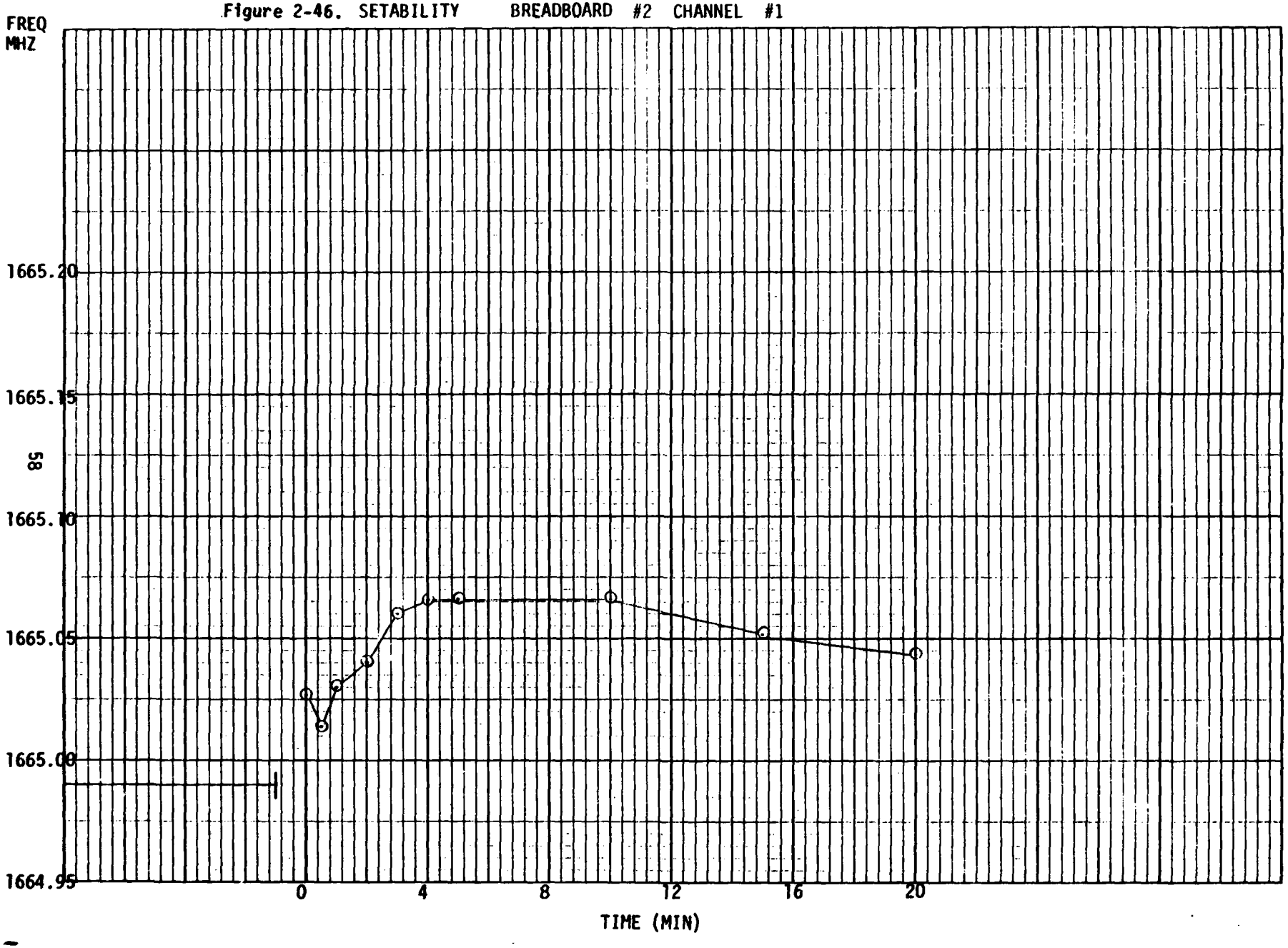


Figure 2-47. FREQUENCY VS TEMPERATURE BREADBOARD #2 CHANNEL #1

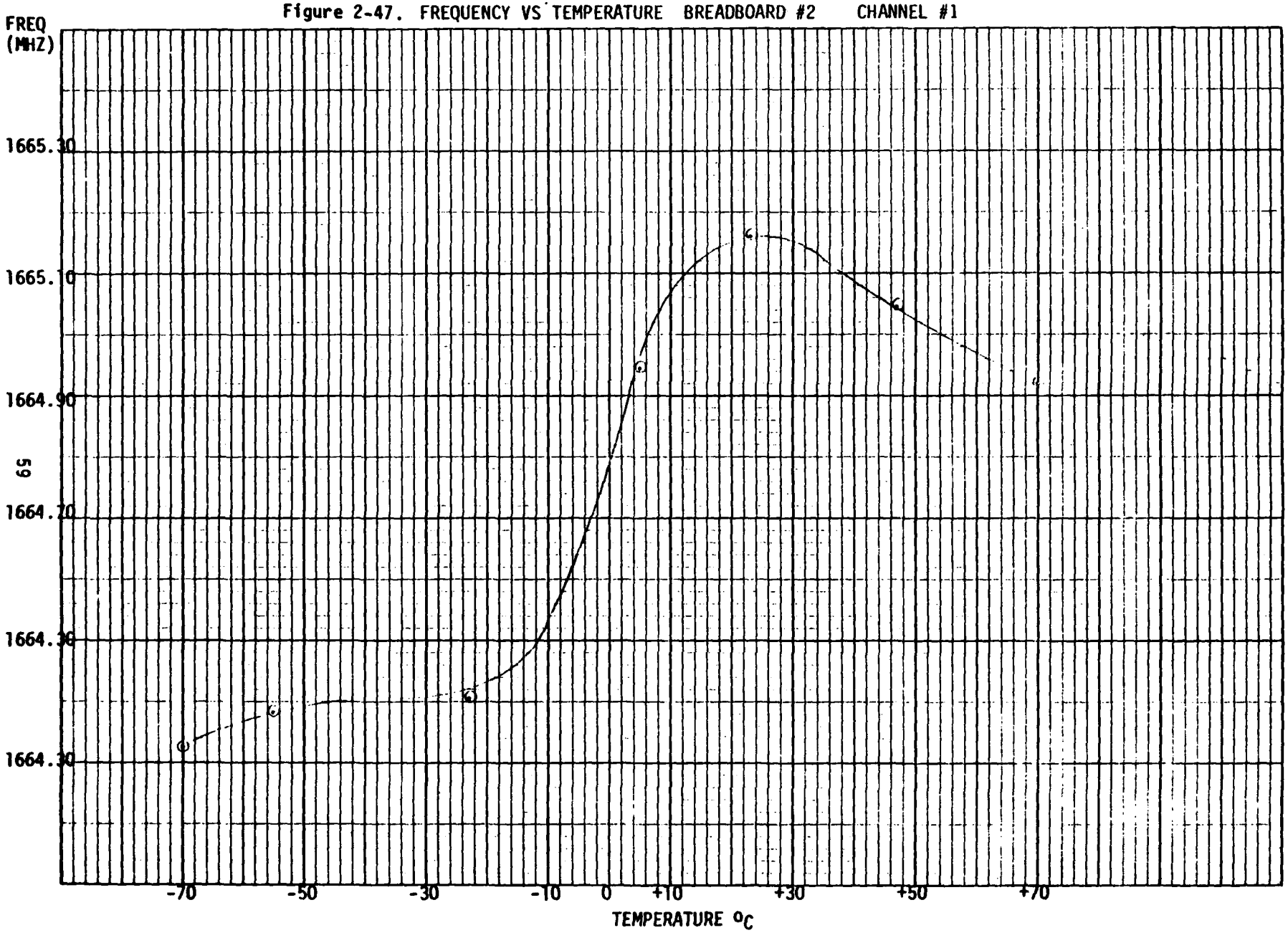


Table 2-4. PERFORMANCE

BREADBOARD #2 CHANNEL #1

A) SPURIOUS LEVELS

FREQUENCY (MHZ)	ORIGIN	P_{OUT} (DBM)	P_{OUT} (DBC)
554.8	SAW FREQUENCY	-22.5	52.0
1110	2X SAW FREQ	-19.0	48.0
3330	2X F_{OUT}	+11.6	17.9
4995.5	3X F_{OUT}	-19.0	48.0

B) FREQUENCY PULLING

ΔF = 1 MHZ ($\pm$500 KHZ) 12 dB RETURN LOSS

C) BIAS

V	$I_{(MA)}$	$P_{(W)}$
13	161.0	2.093
24	116.0	2.784
11.7	132.8	1.554
21.6	100.0	2.160
14.3	161.0	2.302
26.4	136.0	3.590

D) AM (V_{IN} = 1.414V)

P_{ON} = +29.4 dBm

P_{OFF} = -10.0 dBm

Figure 2-48. OUTPUT POWER VS FREQUENCY BREADBOARD #2 CHANNEL #2

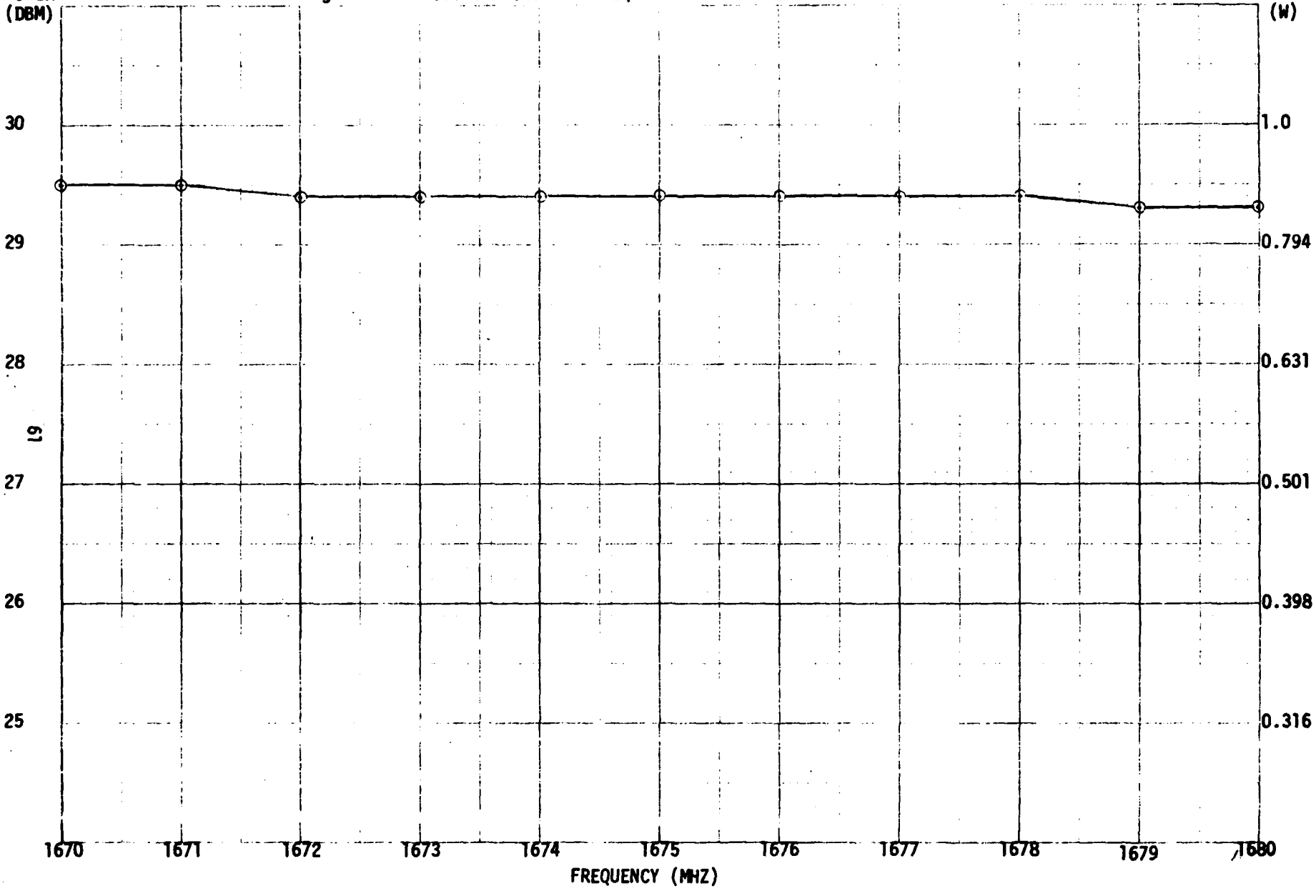


Figure 2-49. SETABILITY BREADBOARD #2 CHANNEL #2

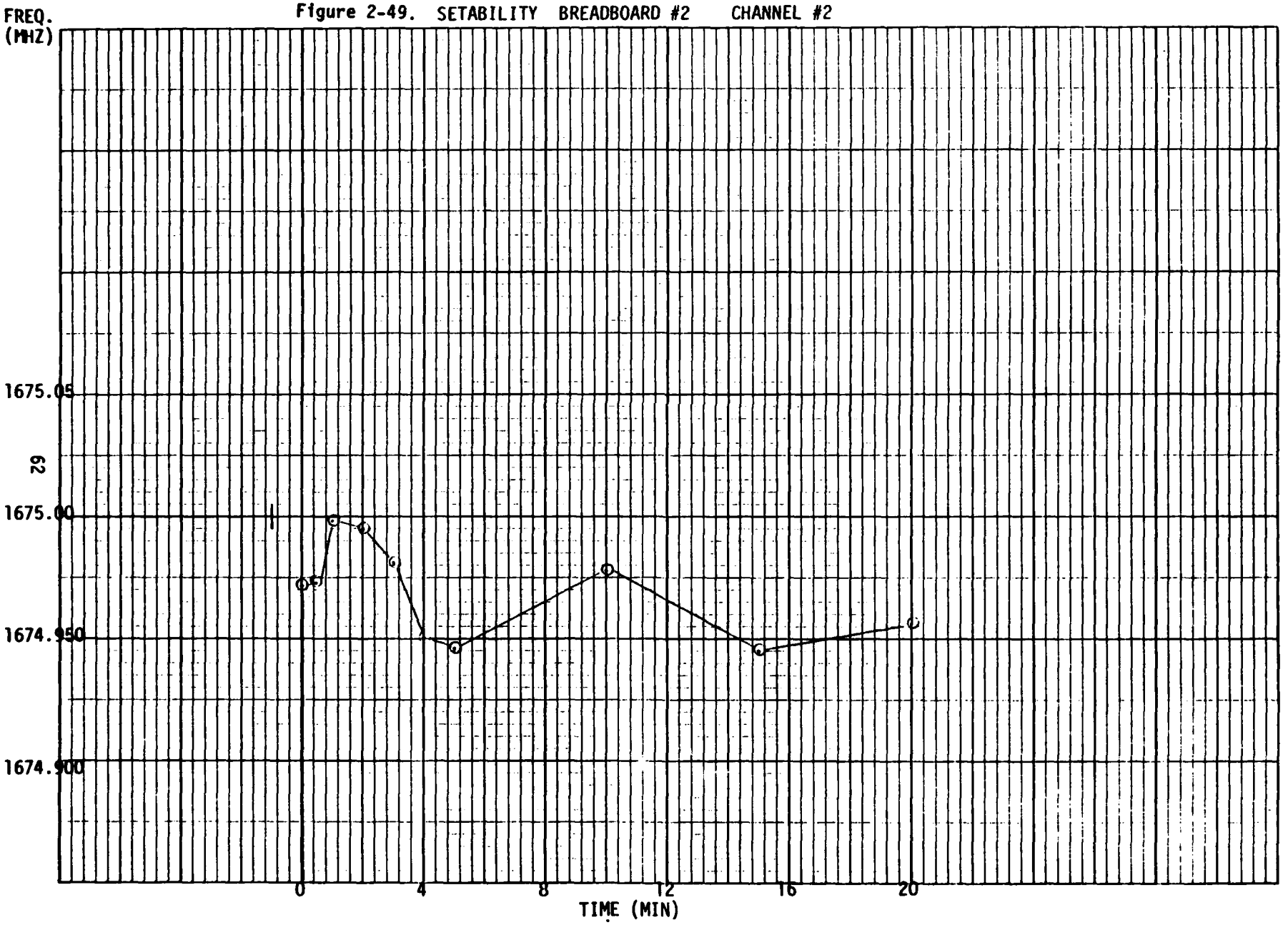


Figure 2-50. FREQUENCY VS TEMPERATURE BREADBOARD #2 CHANNEL #2

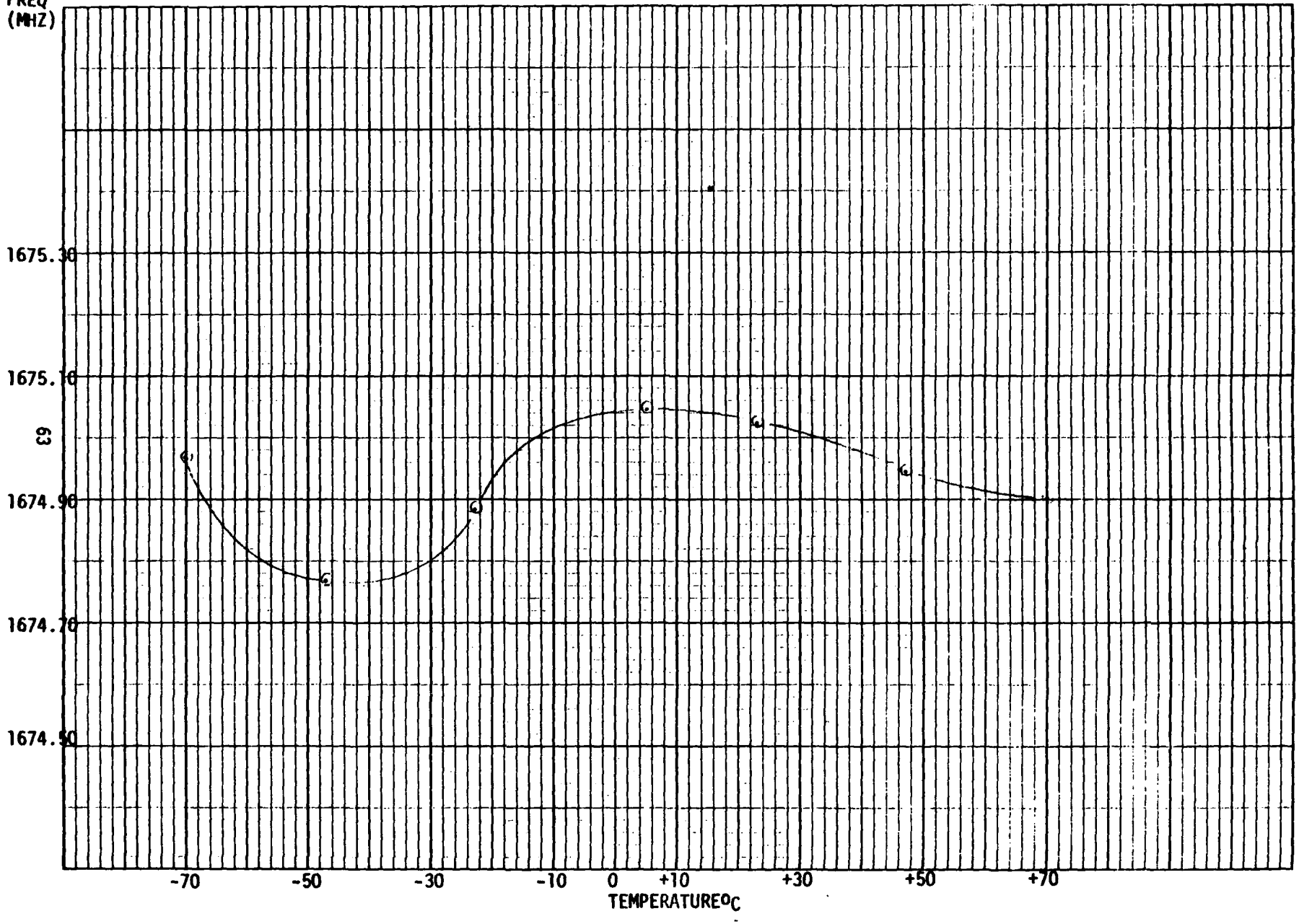


Table 2-5. PERFORMANCE

BREADBOARD #2 CHANNEL #2

A) SPURIOUS LEVELS

FREQUENCY (MHZ)	ORIGIN	P_{OUT} (DBM)	P_{OUT} (DBC)
558.3	SAW FREQUENCY	-27.0	56.4
1116.7	2X SAW FREQ.	-24.0	53.4
3350.0	2X F_{OUT}	+11.5	17.9
5025.0	3X F_{OUT}	-19.0	48.4

B) FREQUENCY PULLING

ΔF = 350 KHz ($\pm$175 KHz) 12 DB RETURN LOSS

C) BIAS

V	$I_{(MA)}$	$P_{(W)}$
13	154.5	2.00
24	111.7	2.68
11.7	124.8	1.46
21.6	90.4	1.95
14.3	152.3	2.18
26.4	128.7	3.40

D) AM (V_{IN} = 1.414V)

P_{ON} = +29.20 dBm

P_{OFF} = -10.00 dBm

Figure 2-51. OUTPUT POWER VS FREQUENCY BREADBOARD #2 CHANNEL#3

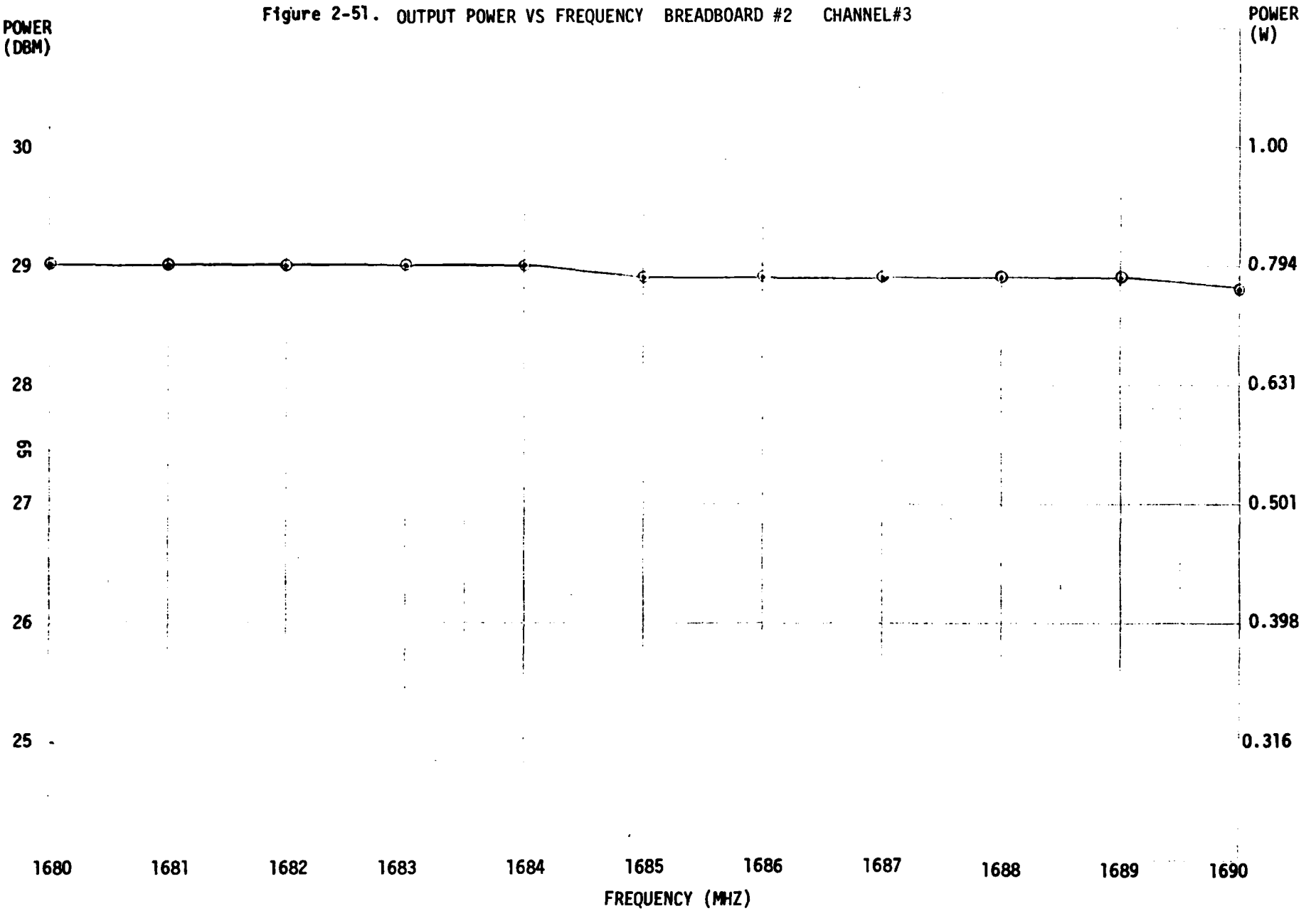


Figure 2-52. SETABILITY BREADBOARD #2 CHANNEL #3

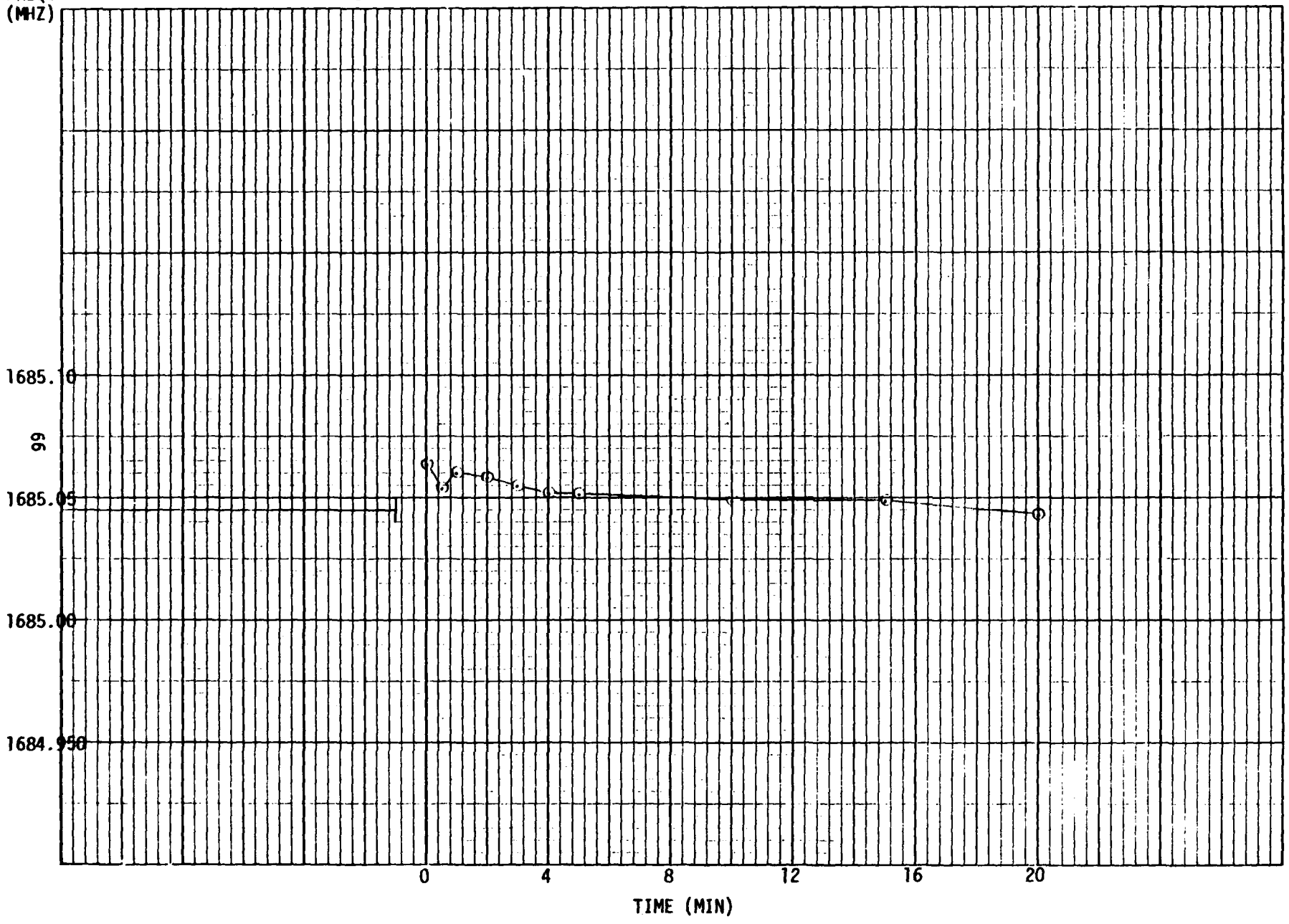


Figure 2-53. FREQUENCY VS TEMPERATURE BREADBOARD #2 CHANNEL #3

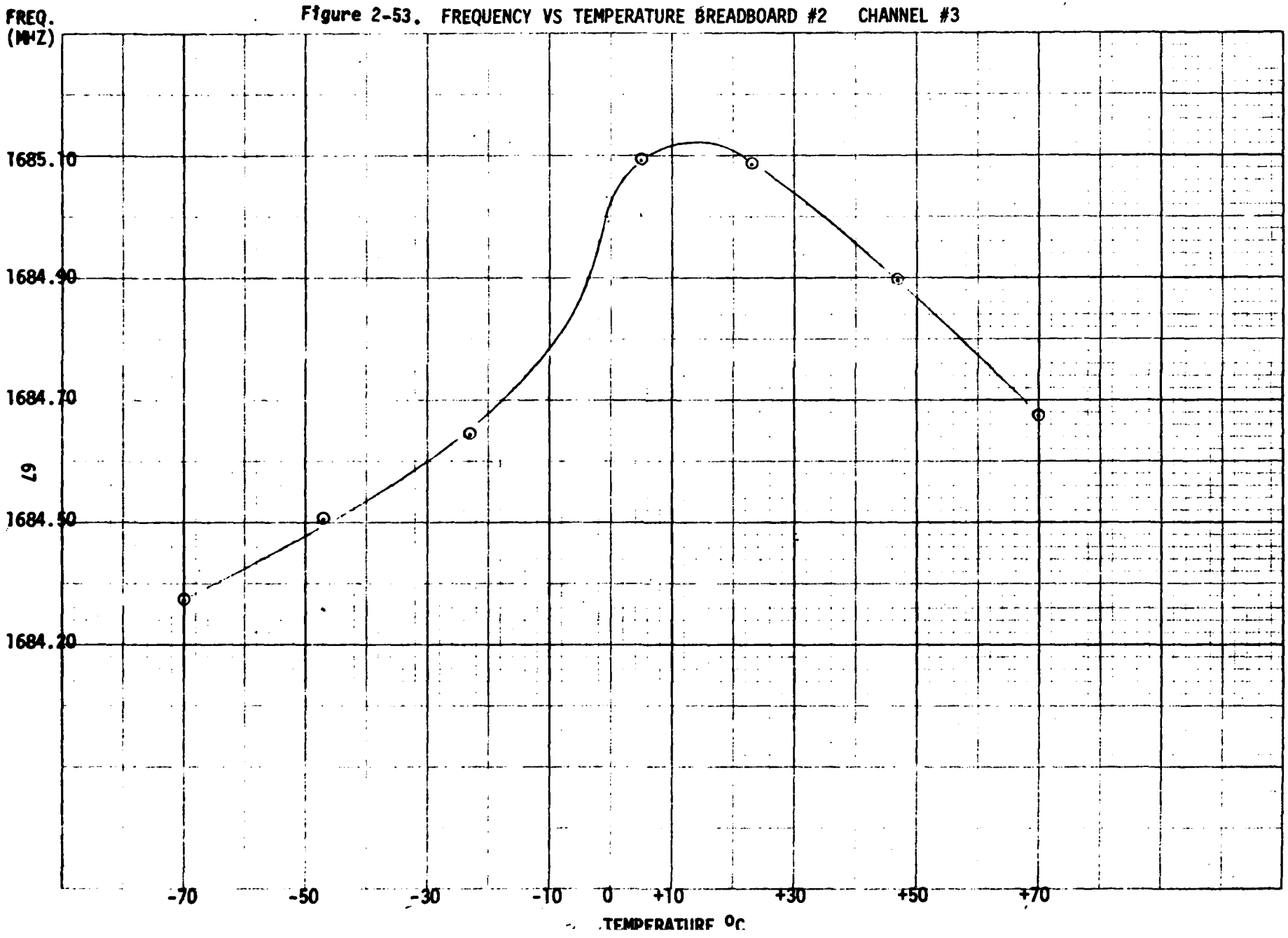


Table 2-6. PERFORMANCE

BREADBOARD #2 CHANNEL #3

A) SPURIOUS LEVELS

FREQUENCY (MHZ)	ORIGIN	P_{OUT} (DBM)	(DBC)
561.65	SAW FREQUENCY	-19	48.00
1123.38	2X SAW FREQ	-16.8	45.80
2246.80	4X SAW FREQ	-15.5	44.50
3370.15	2X F_{OUT}	+10.9	18.10

B) FREQUENCY PULLING

ΔF = 450 KHZ ($\pm$225 KHZ) 12 dB RETURN LOSS

C) BIAS

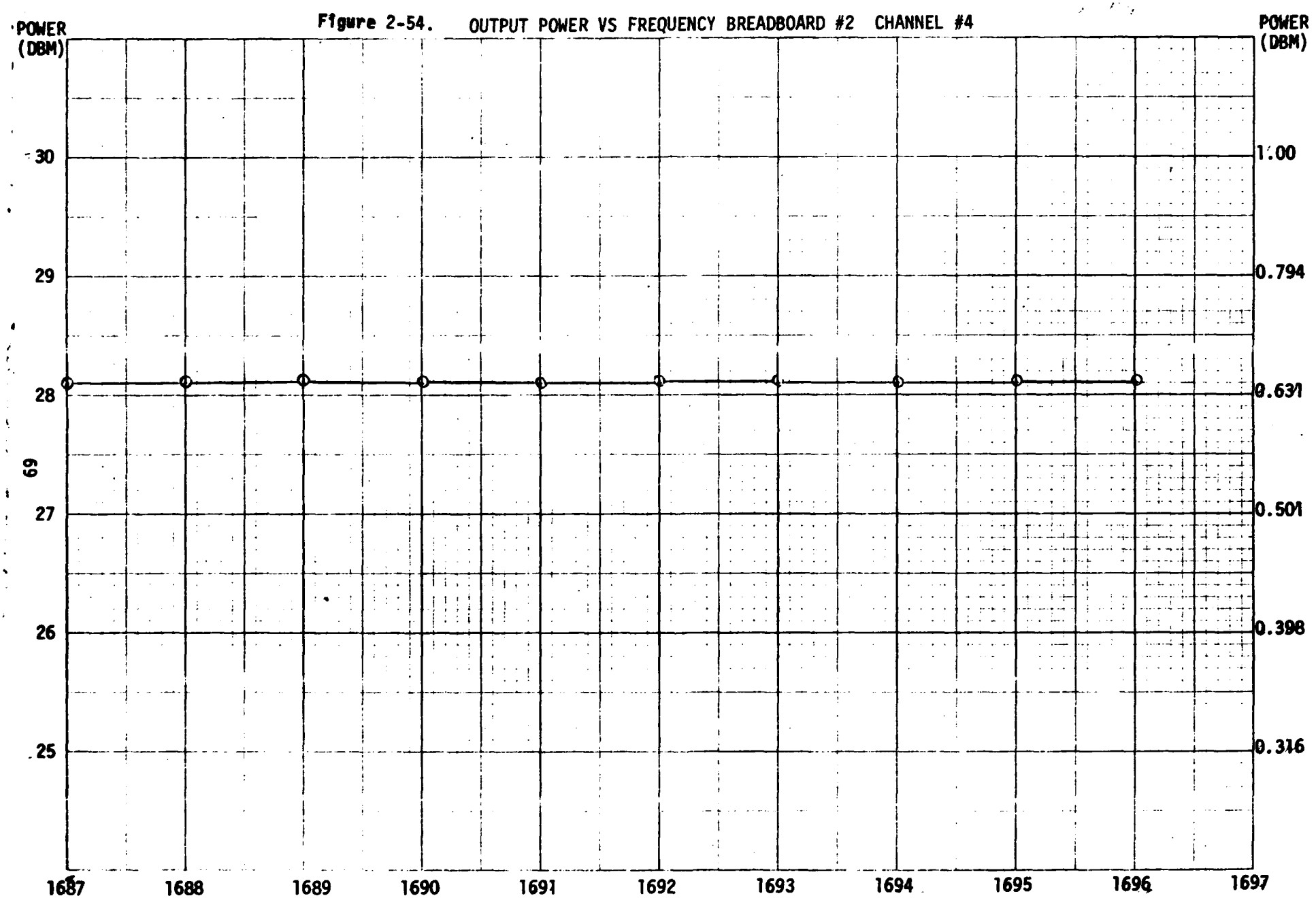
V	$I_{(MA)}$	$P_{(W)}$
13	180.0	2.340
24	99.6	2.390
11.7	140.6	1.645
21.6	86.1	1.860
14.3	184.2	2.634
26.4	117.26	3.096

D) AM (V_{IN} = 1.414 V)

P_{ON} = +29.0 dBm

P_{OFF} = -10.0 dBm

Figure 2-54. OUTPUT POWER VS FREQUENCY BREADBOARD #2 CHANNEL #4



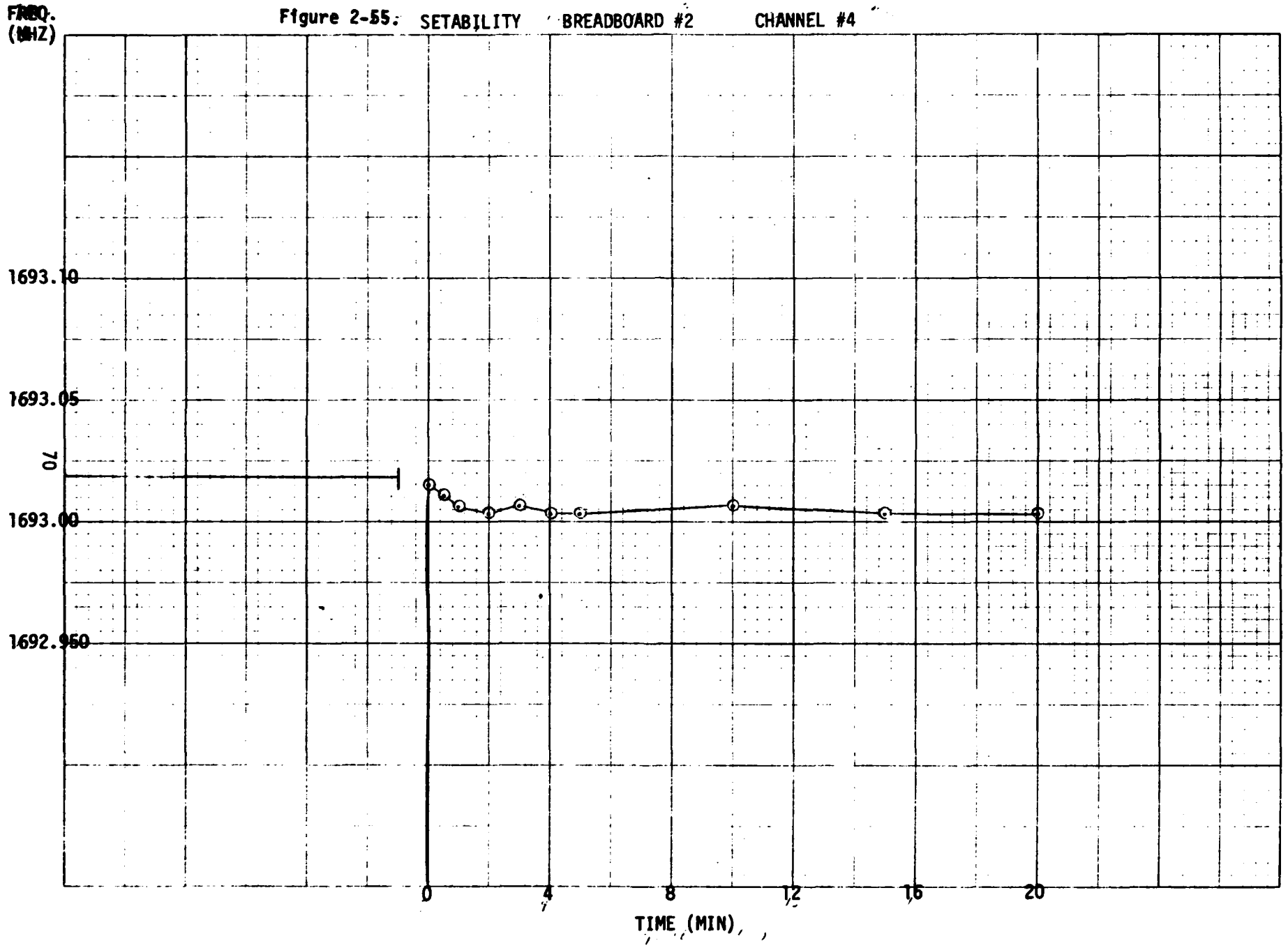


Figure 2-55. SETABILITY BREADBOARD #2 CHANNEL #4

Figure 2-56. FREQUENCY VS TEMPERATURE BREADBOARD #2 CHANNEL #4

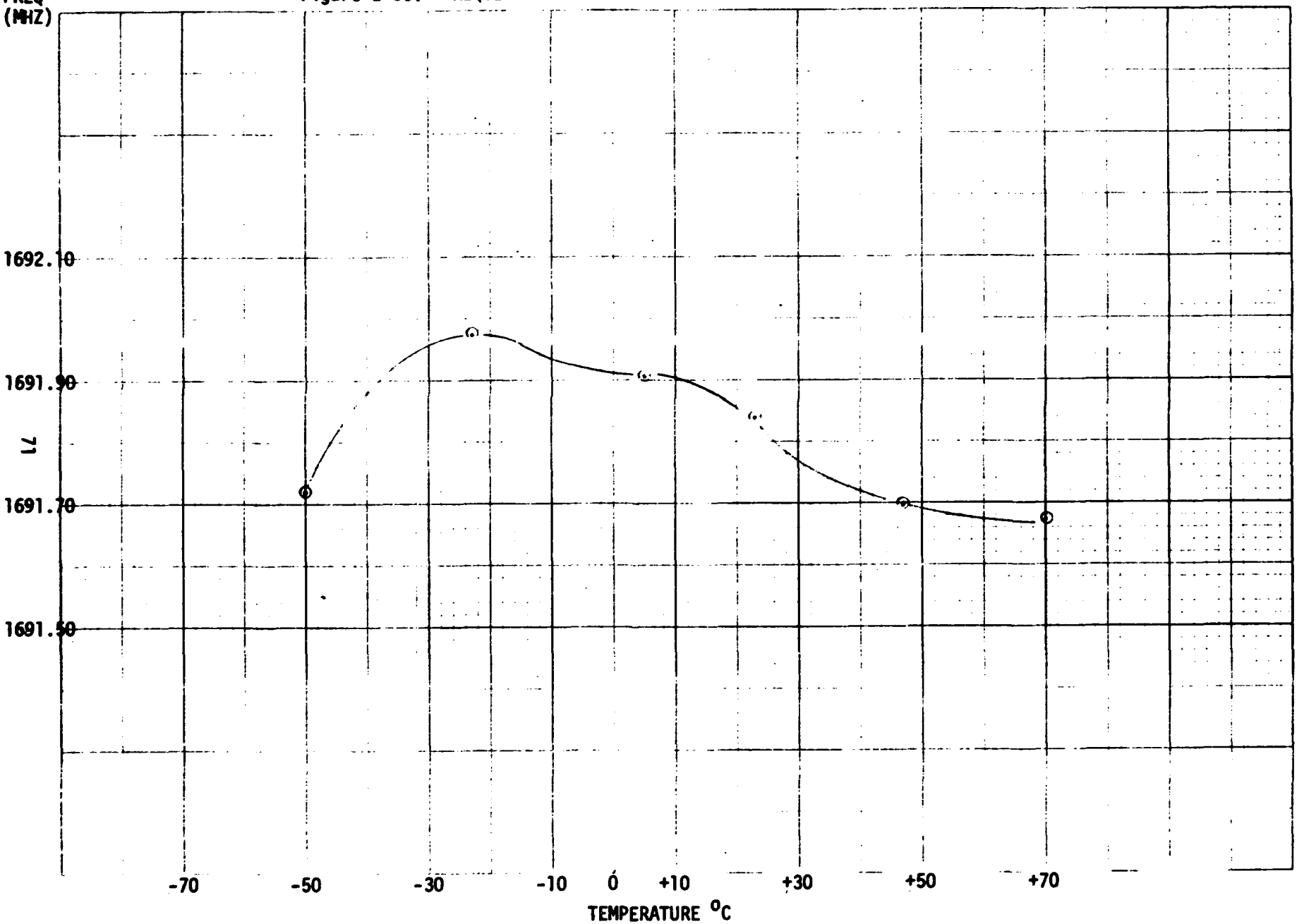


Table 2-7. PERFORMANCE

BREADBOARD #2 CHANNEL #4

A) SPURIOUS LEVELS

FREQUENCY (MHZ)	ORGIN	P_{OUT} (dBm)	(dBc)
564.36	SAW FREQUENCY	-17.60	45.70
1128.79	2X SAW FREQ.	-17.50	45.60
2257.47	4X SAW FREQ	-17.60	45.70
3386.17	2X F_{OUT}	+10.30	17.80

B) FREQUENCY PULLING

ΔF = 300 KHZ ($\pm$150 KHZ) 12 dB RETURN LOSS

C) BIAS

V	I (MA)	P(W)
13	175.7	2.284
24	82.6	1.982
11.7	150.7	1.763
21.6	69.7	1.506
14.3	132.4	1.893
26.4	93.4	2.466

D) AM (V_{IN} = 1.414V)

P_{ON} = +28.0 dBm

O_{OFF} = -20.4 dBm

Table 2-8. TEMPERATURE STABILITY OF BREADBOARD OSCILLATOR NO. 2

BREADBOARD OSCILLATOR #2	CHANNEL #	TEMP. ^{o}C	FREQ MHZ	P_{OUT} (DBM)	f (PPM)
	1	+70	1664.921	+28.00	501
		+23	1665.161	+28.00	
		-70	1664.326	+28.10	
	2	+70	1674.900	+27.80	159
		+ 5	1675.045	+27.80	
		-47	1674.779	+27.90	
		-70	1674.968	+27.90	
	3	+70	1684.678	+27.80	486
		+ 5	1685.094	+27.80	
		-70	1684.274	+27.70	
	4	+70	1691.673	+28.00	178
		-23	1691.975	+28.00	
		-50	1691.721	+26.20	

3. FREQUENCY SYNTHESIZER

The requirements for the frequency synthesizer, as described in the contract statement-of-work, are shown in Table 3-1. Based on the JTIDS system study which is described in detail in the first interim report, the requirements for a JTIDS class 3 frequency synthesizer are shown in Table 3-2. The current synthesizer design is based on meeting the objectives defined in Table 3-1, with the exception of the frequency range, which shall be 1296-1533 MHz. It is also felt that the power goal of 5W will be extremely difficult to meet. In fact, our current estimate is a power consumption of 9.5W, which could be lowered to perhaps 7W with the optimization of the RF/LSI chips.

a. System Architecture

Figure 3-1 is a detailed block diagram of the synthesizer architecture. The design utilizes a mix-and-divide scheme whereby four mix-and-divide monolithic RF/LSI chips are used to switch, divide, and add or subtract three selectable frequencies to provide the required output tones.

An external reference source of 40.5 MHz is used to lock the three SAW oscillators. The reference is also used to injection lock the reference 486 MHz SAW oscillator. This provides frequency coherency for the synthesizer. If such coherency were not required, an obvious simplification would to to allow the SAW oscillators to be free-running oscillators. The 526.5, 567, and 607.5 MHz SAW oscillators are filtered by a single stage bank of SAW filters which have the effect of eliminating the undesired tones present because of the injection locking signal. These filter outputs are then selected by their respective RF/LSI chips. Each RF/LSI circuit consists of two chips comprising driver, an amplifier, a frequency divider, and an analog multiplier (mixer).

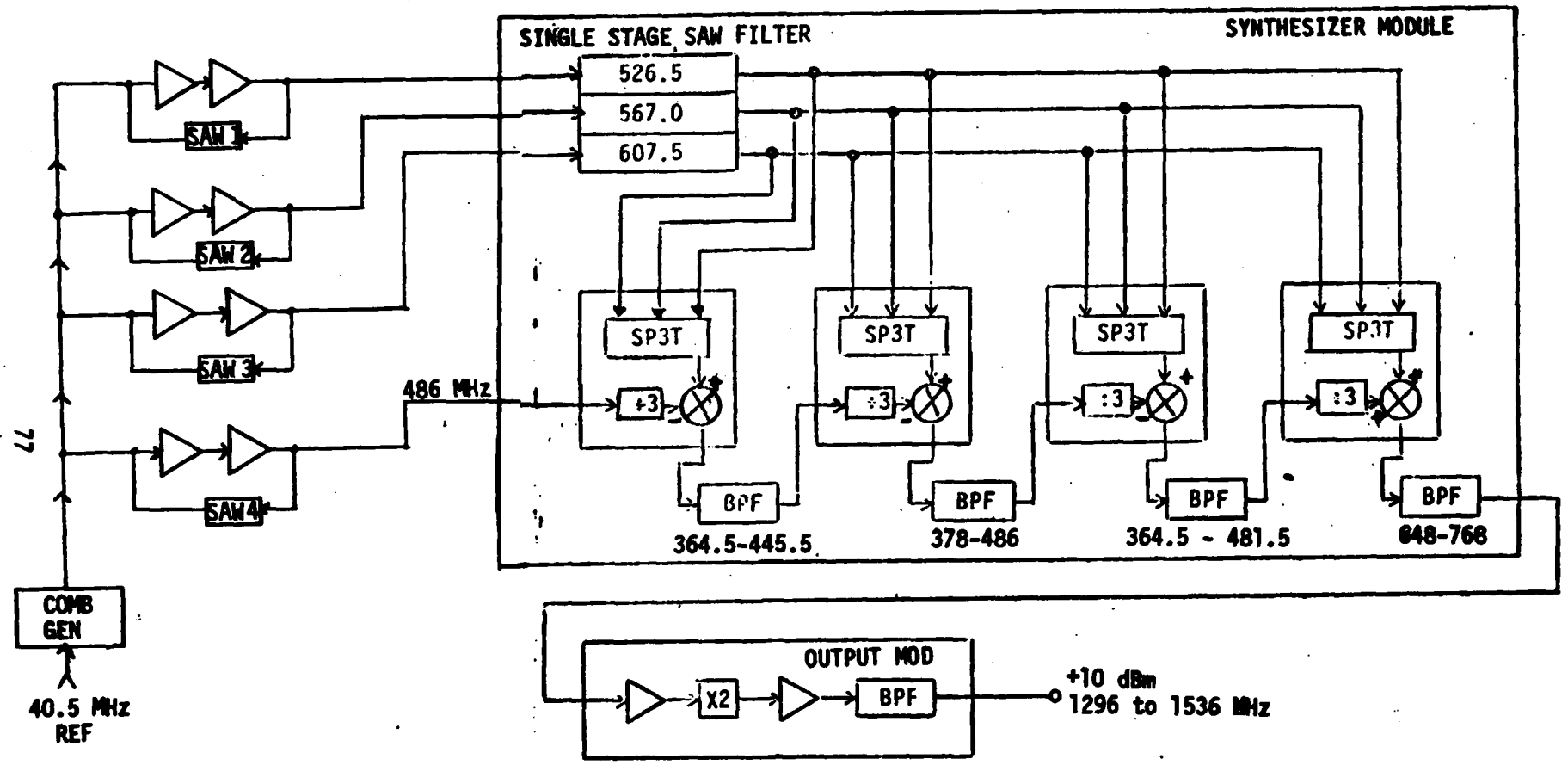
Table 3-1. CONTRACT SPECIFICATIONS

Parameter	Requirement
Frequency Range	950-1202 MHz
Step Size	3 MHz
Spurious Suppression	-68 dBc
Frequency Stability	1×10^{-9}/sec 1×10^{-8}/month
Phase Noise	65 dBc/Hz @100 Hz Offset 80 dBc/Hz @ 1 KHz Offset >120 dBc/Hz @ Noise Floor
Switching Speed	<1.0 μs
Settling Time	<0.1 μs
Output Level	10 dBm ± 1 dBm
Size	10 $in.^3$
Power	<5W
Voltages	N/S
Digital Control Levels	N/S

Table 3-2. JTIDS REQUIREMENTS

Parameter	Requirement
Frequency Range	1296-1533 MHz
Step Size	3 MHz
Spurious Suppression	-64 dBc @ 1296-1327 -42 dBc @ 1347-1352, 1362-1367, 1407-1412, 1422-1427 -62 dBc @ 1352-1354, 1360-1362, 1412-1414, 1420-1422 -82 dBc @ 1357 ±3 and 1417 ±3 -40 dBc @ rest of band
Frequency Stability	$\pm 1 \times 10^{-5}$ (approximately ±15 KHz)
Phase Noise	60 dBc/Hz@ 100 Hz 74 dBc/Hz @ 1 KHz >120 dBc/Hz @ Noise Floor
Settling Time	200 nS
Output Level	10 dBm
Size	10 $in.^3$
Power	<5W
Voltages	+5V, ±15V
Digital Control Levels	TTL

FIGURE 3-1. SYNTHESIZER WITH INDEPENDENT SAW OSCILLATORS



On the last three chips, when one of the three frequencies is chosen, it is mixed with the output of the previous chip which has been filtered, amplified, and divided by 3. On the first chip the selected frequency is mixed with 162 MHz, derived from the output of the phase-locked loop by dividing by 3. In this fashion, each chip provides several possible output tones: the first outputs from 364.5 to 445.5 in 40.5 MHz steps; the second from 378 to 486 in 13.5 MHz steps; the third in 4.5 MHz steps from 367.5 to 481.5 MHz; and finally, 1.5 MHz steps are provided from 648 to 768 MHz. When this output is multiplied by 2, the desired 3 MHz steps from 1296 to 1536 MHz are generated. It should be noted that on all but the last chip, the difference frequency in the mixer is selected.

Frequency selection is provided by controlling the switches. Due to the fact that subtraction is used, the algorithm becomes complex. Since 3 MHz steps are employed, and each switch is an SP3T, a base 3 number system is indicated to provide the algorithm. Let the switches be numbered, from the left, as 0, 1, 2, 3, and in switches 0, 2 and 3 let 0 select 526.5, 1 select 567, and 2 select 607.5 In switch 1, the reverse order must be used: 0 must select 607.5, 1 must select 567, while 2 selects 526.5. To select a desired frequency, n must be determined, where n is given by

$$f_{desired} = 1296 + 3n$$

or

$$n = \frac{f_{desired} - 1296}{3}$$

Next n is converted from base 10 to base 3. The switch position for each switch is given by this number, according to the switch number and the column number.

For example, suppose the desired frequency is 1389 MHz. This means n=31. In base 3 this number becomes 1011. According to the algorithm, switches 0, 1, and 3 are set to 567 and switch 2 is set to 526.5. If those numbers are run through the operations indicated in Figure 3-1, we find that the output frequency is 1389 MHz.

b. Frequency Source Generation

The current architecture of the frequency synthesizer differs from the design discussed in the previous interim report, which is shown for reference in Figure 3-2. The differences are primarily in the generation of the 526.5, 567, and 607.5 MHz frequencies. Several approaches were considered in addition to the multimode locked SAW oscillator discussed previously. These are the injection locked SAW oscillator approach discussed in Figure 3-1 (our current baseline) and dual phase-locked-loop/multitone generator approach. Table 3-3 summarizes the comparison of these methods of generating the desired sources.

The dual PLL/multitone generator approach is shown in Figure 3-3. It consists of two phase-locked-loop chips to generate the 526.5 and 567 MHz tones, and by passing through a nonlinear amplifier device its intermodulation products can be used to generate the 607.5 MHz tone. However, this method consumes considerably more power (approximately 1W more) and does not utilize SAW devices.

The major difficulty with the multimode locked SAW oscillator (MLSO) approach is an injection locking problem. The MLSO shown in Figure 3-2 was breadboarded and characterized and injection locking properties investigated This investigation has led to an understanding of multimode oscillators which differs from that discussed in the literature.[1,2] Measurements

[1] M. Gilden, T.M. Reeder, A.J. Demaria, "The Mode-Locked SAW Oscillator", Ultrasonics Symposium Proceedings, 1975, pp. 251-254.

[2] M. Gilden, "Stablilized SAW Comb Spectrum Generators", Ultrasonics Symposium Proceedings, 1977, pp. 1-5.

FIGURE 3-2. SYNTHESIZER WITH MLSO

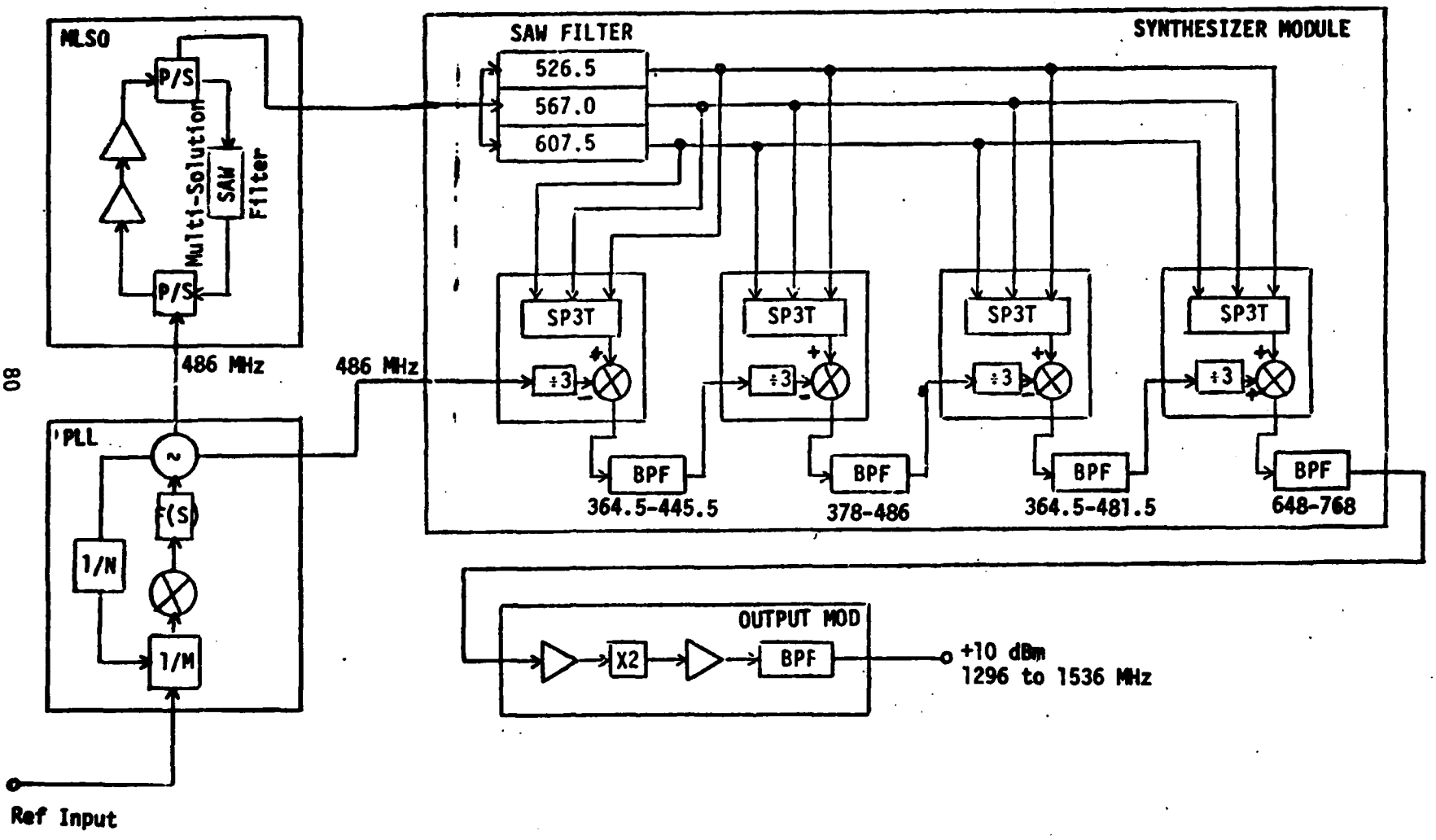


TABLE 3-3.

COMPARISON OF FREQUENCY SOURCE GENERATOR

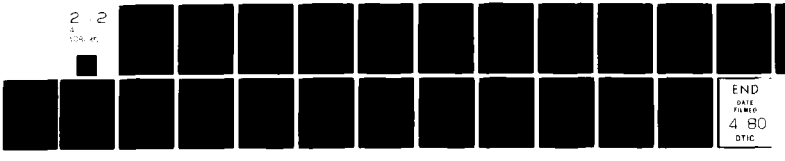
TYPE: (TONE GENERATOR)	DC POWER	SIZE	RISK	COMMENTS
INJECTION LOCKED SAW OSCILLATORS	9.5W*	11 CU. IN.	LOW	OPTION OF FREE RUNNING OSCILLATION
MULTIMODE LOCKED SAW OSCILLATOR	10W*	13.5 CU. IN	HIGH	INJECTION LOCKING PROBLEM
DUAL PLL/MULTIMODE GENERATOR	10.5W*	14.5 CU. IN.	LOW	AMPLIFIER POWER COMPOSITION

* RF/LSI DESIGN MODIFICATIONS ARE REQUIRED TO LOWER POWER.

AD-A082 351 TRW DEFENSE AND SPACE SYSTEMS GROUP REDONDO BEACH CA F/G 9/5
SURFACE ACOUSTIC WAVE MICROWAVE OSCILLATOR AND FREQUENCY SYNTHE--ETC(U)
JAN 80 M Y HUANG, D J DOOSON DAAB07-78-C-2992

UNCLASSIFIED DELET-TR-78-2992-2 NL

2 2



END
DATE FILMED
4 80
DTIC

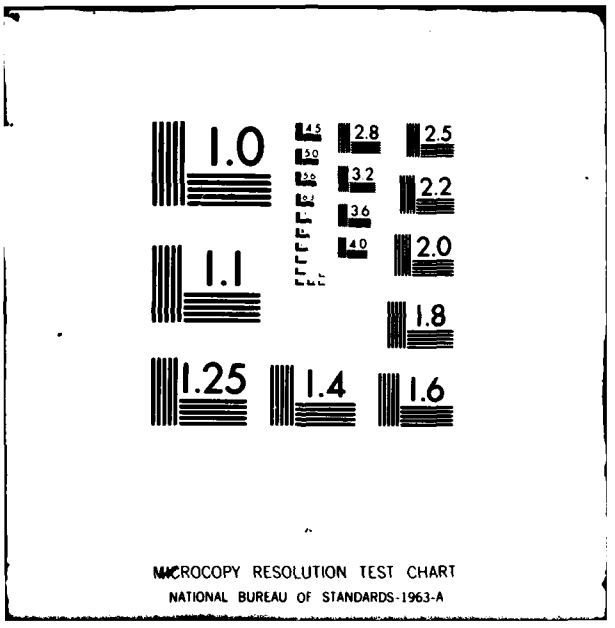
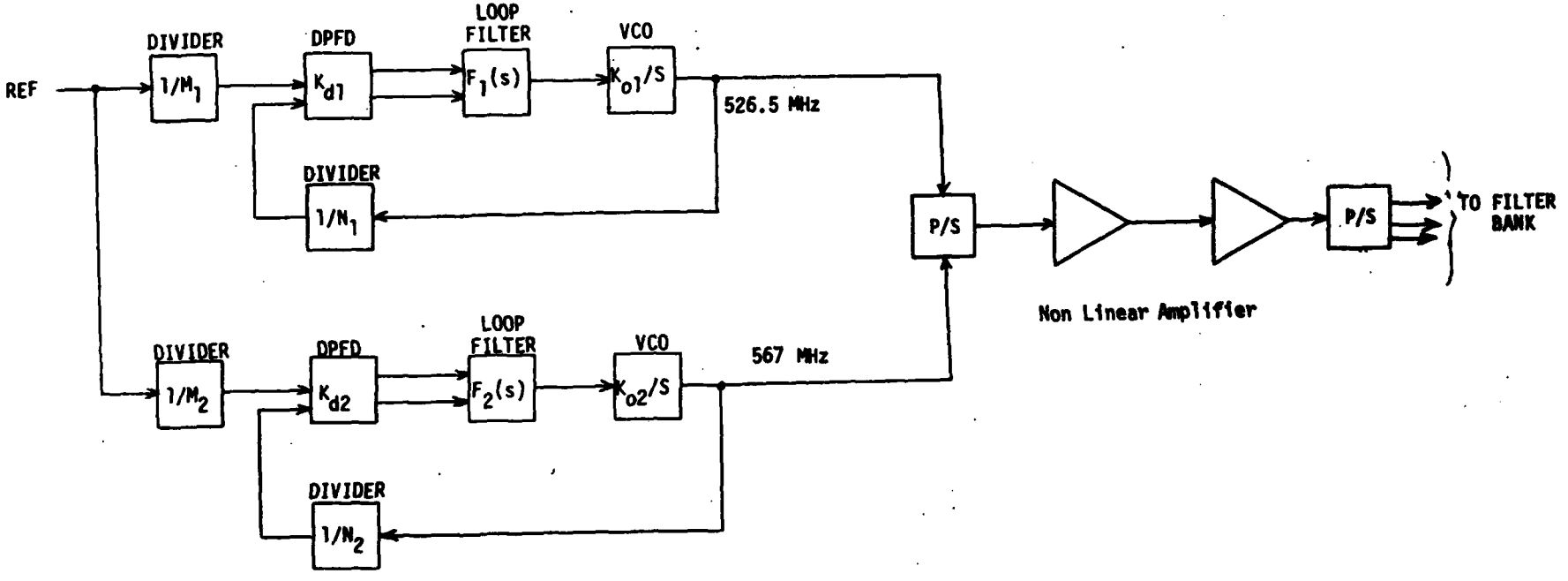

1.0
1.1
1.25
1.4
1.6
1.8
2.0
2.2
2.5
2.8
3.2
3.6
4.0
MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

FIGURE 3-3. Dual PPL, MTG Circuitry



M_i = Reference divider ratio

N_i = VCO divider ratio

K_{di} = detector gain (volts/rad)

K_{oi} = VCO gain ($\frac{rad/sec}{volt}$)

F(s) = filter response (volt/volt)

indicate that multimode oscillations result from the generation of intermodulation products in the circuit non-linearities. For proper frequency ratios, the intermodulation products add energy to the loop at frequencies of oscillation which are normally suppressed, and thereby maintain oscillations at more than one frequency. One line of evidence which supports this view resulted from the construction of a multimode oscillator using tunable BPFs as shown below.

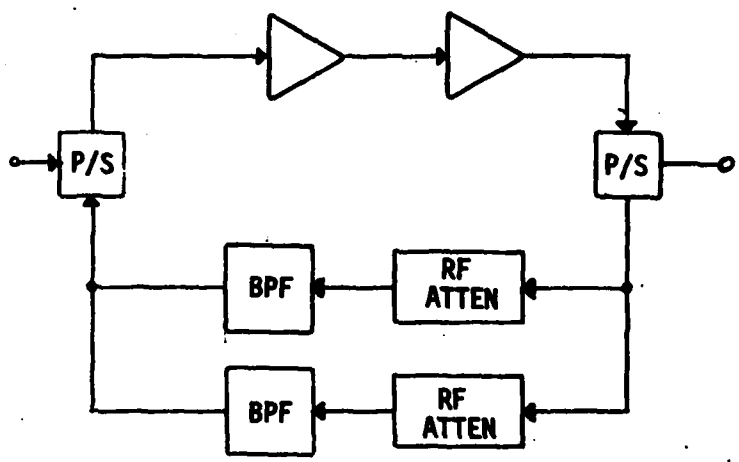


Figure 3-4. Dual Passband Oscillator

The circuit demonstrated multimode oscillations when the filters were set such that IM products of the two possible frequencies of oscillation fell in the filter passbands. Multimode oscillations did not generally occur when this was not the case. When multimode oscillations were present each

output frequency could be identified as a harmonic or an IM product of the two passband frequencies.

Injection locking tests on a breadboard MLSO indicated that the 4 output frequencies could not simultaneously be injection locked to a single input frequency. The breadboard utilized a multi-passband SAW filter with filter passbands at 480, 512, 544, and 576 MHz. Tests were performed with injection locking frequencies of 480, 512, 544, 576 and 32 MHz. In no case did the four outputs become simultaneously locked to the input. The results of the injection locking tests are briefly summarized in the table below. The table shows the relative change in the output frequencies vs change in injection locking frequency ($\Delta f_{OUT}/\Delta f_{INj}$) for four injection locking frequencies.

Table 3-4. INJECTION LOCKED TEST DATA

	$\Delta f_{OUT}/\Delta f_{INj}$			
f_{INj} (MHz)	480	512	544	576
480	1.0	∿.61	∿0	∿0
512	∿1.66	1.0	∿0	∿0
544	∿2.66	∿1.85	1.0	∿0
576	∿-2.33	∿-1.25	∿0	1.0

This data suggests that the frequencies most likely to free run in this loop are the 544 MHz and 576 MHz. The other tones are likely sustained by IM products of these two. Possibly 480 MHz is obtained by 3(544 MHz)-2(576 MHz), and 512 MHz by 2(544 MHz) - 576 MHz. Since stability of the reference tones could not be derived by injection locking one of the modes, the injection locked SAW oscillator approach was selected as the baseline design.

The injection locked SAW oscillator approach consists of generating a comb of frequencies from the reference 40.5 MHz. This signal is then introduced to each of four free-running SAW oscillators at 486, 526.5, 567, and 607.5 MHz, as shown in Figure 3-1. Preliminary experiments have indicated that when these tones are inserted at a low power point, a relatively low power tone can be used for injection lock. The problem with this technique is that the adjacent tones which are not injection locked will appear as spurious components to the desired frequency. Therefore, additional filtering after the SAW oscillator is required to reject the unwanted components to 70 dB. Because these spurious components are expected to be 30-40 dB below the desired signal, an easily obtainable low sidelobe SAW filter should be all that is required. Work is currently in progress on the design of the RF/LSI chips and the SAW filters.

c. RF/LSI Design

Because of the very stringent isolation requirements and to allow for maximum flexibility in the testing and investigation of the synthesizer, the LSI chip design has been segregated into two functions; that of the switch and that of the divide-and-mix function. An SP4T switch (rather than an SP3T switch) and a universal ÷3/÷4 (user selectable) divide and mix was designed.

(1) SP4T Switch

The SP4T switch provides 70 dB of isolation of the unselected inputs relative to the selected input, as measured at the switch output. This is a difficult requirement, and a number of features are being included in the circuit design to specifically address the isolation problem. To avoid coupling through power supply or ground impedances, all circuitry is differential. The input signal as supplied is single ended, so the complimentary side of each differential input is brought out and grounded at the ground terminal of the transmission line supplying that input. Also, the selected channel has gain,

so that less attenuation is required in the channels not selected. Power supplies are +5 volts for VCC and-5 volts for VEE. The select inputs accept TTL levels between 0 and +5 volts. The overall block layout of the SP4T switch is shown in Figure 3-5.

Figures 3-6 through -10 show the block diagram and detailed schematics for each section of the circuit. Note that the four switch input sections (Figure 3-9) have a differential connection to the output section, and each has its own power supply connections. The output section (Figure 3-10) also has its own power supply connections. In this manner, stray coupling is reduced since signal currents in power supply lines do not have common bond wire and package lead impedances.

When the switch channel shown in Figure 3-9 is selected, the select input is pulled low, allowing the current sources for the differential pairs to be turned on. In the on state, the selected signal is amplified through two differential common-emitter/common-base cascade stages. The first stage includes diode peaking to flatten the overall frequency response. The gain is stabilized by emitter degeneration resistors and should be about 20 dB overall in the selected channel. The second common-base stage serves also to combine the channels. In the off state, the isolation from input to output is primarily obtained from the two common-base stages, which have provision to reverse-bias their emitter-base junctions when they are not selected. It is assumed that both the inputs and the output will be capacitor coupled.

Input impedance of a switch should be in excess of 200 ohms exclusive of the package capacitance. A level of -40 dBm at the input should provide -20 dBm at the output to drive the mixer; to allow some margin in design, the provisional system specification will provide -35 dBm at the switch input.

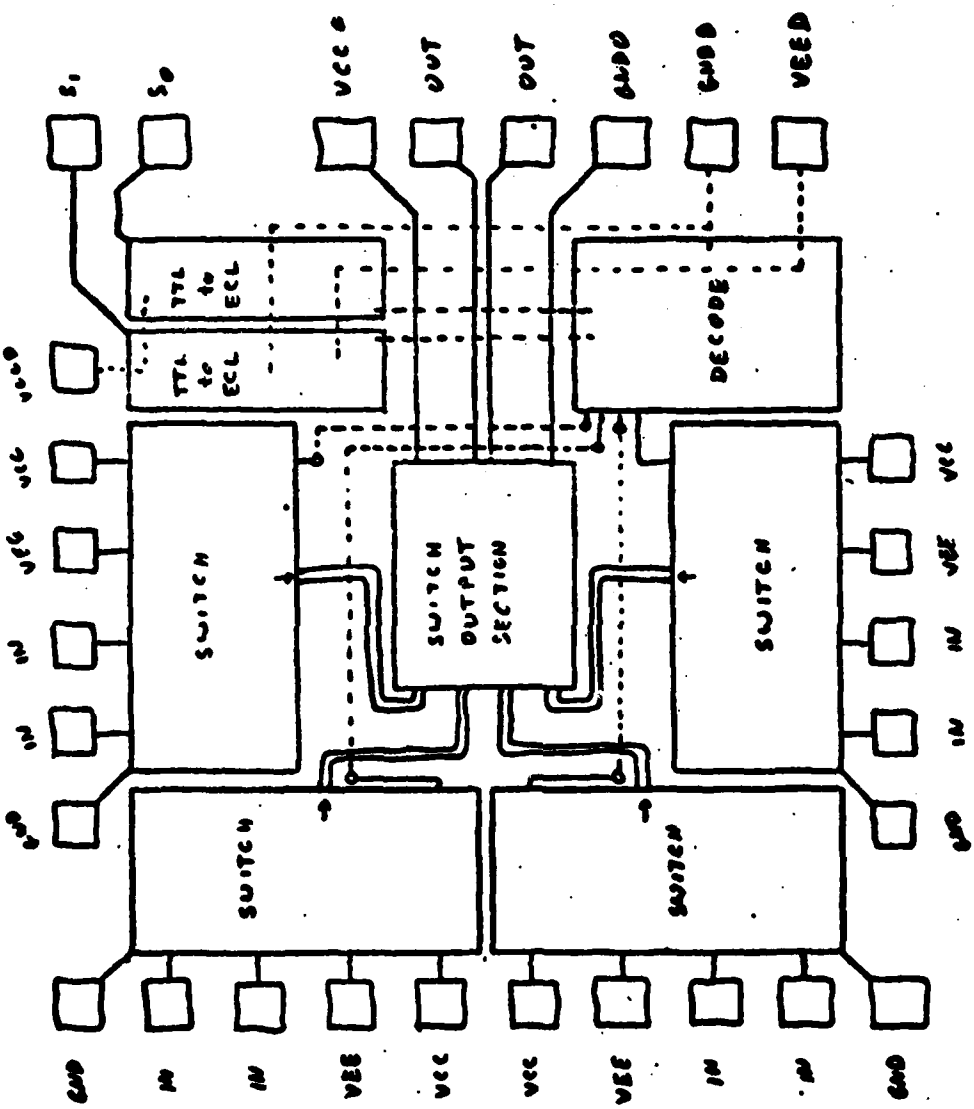


Figure 3-5. SP4T SWITCH PRELIMINARY BLOCK LAYOUT

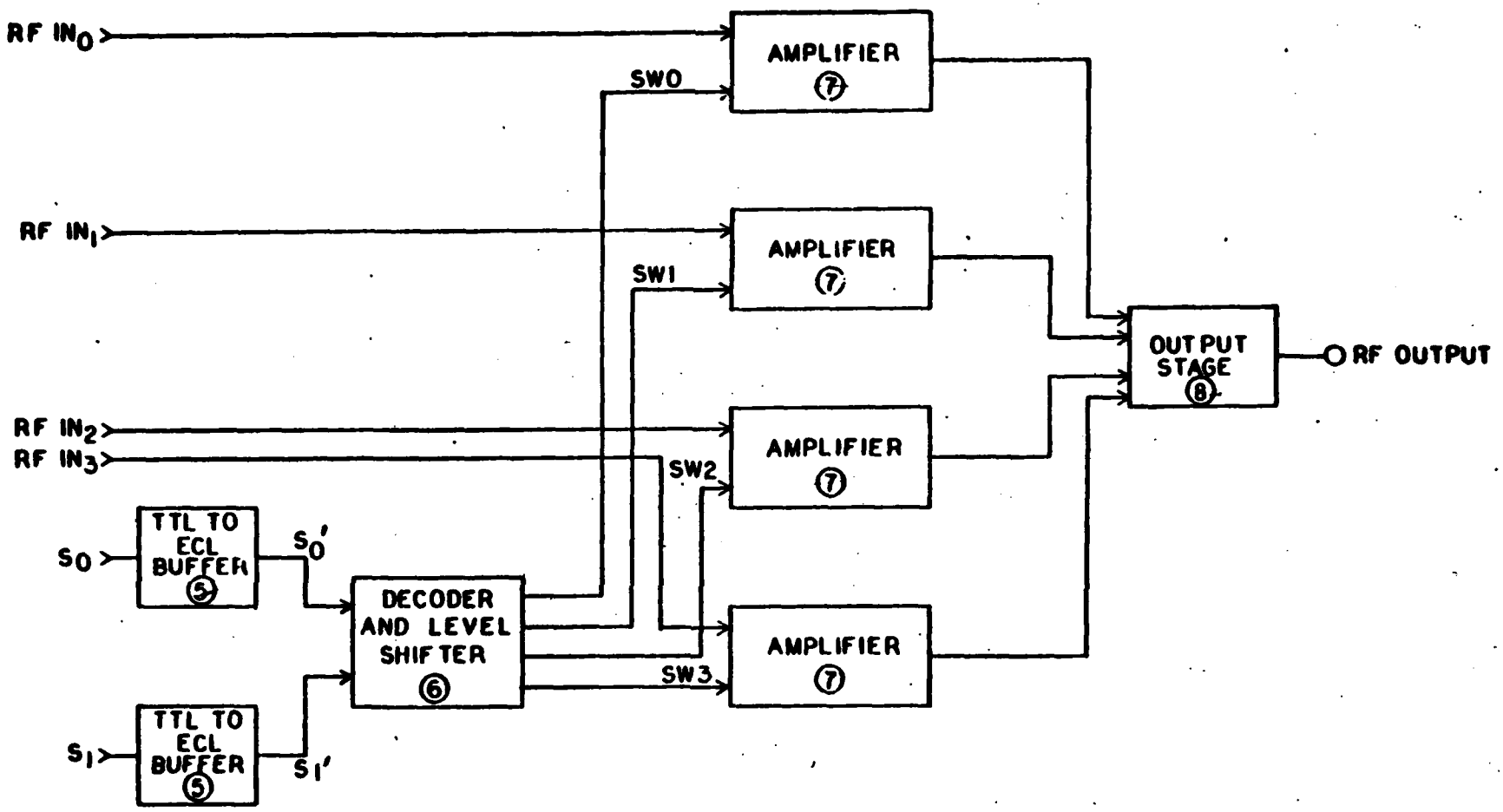


Figure 3-6. RF SWITCH BLOCK DIAGRAM

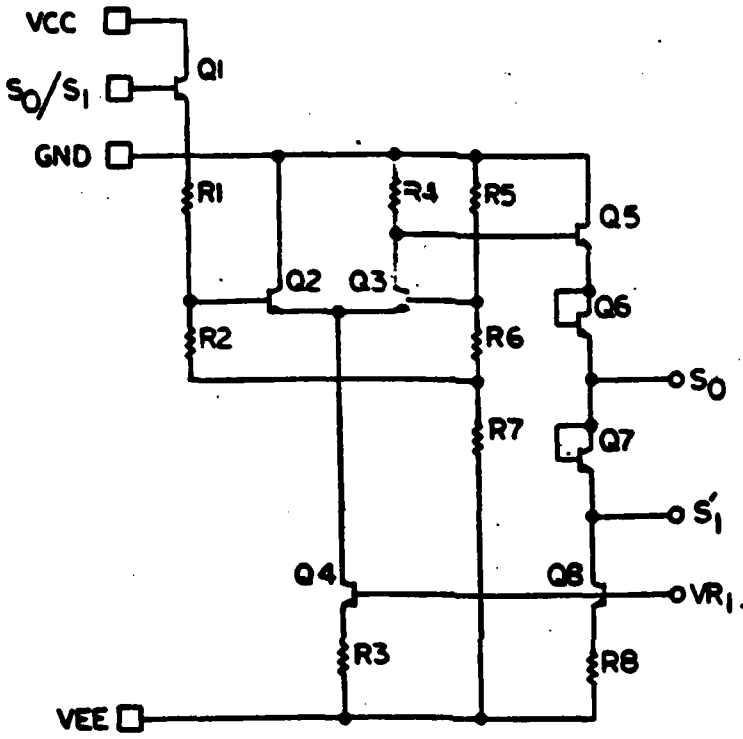


Figure 3-7. R.F. SWITCH TTL TO ECL BUFFER

RESISTOR VALUES ARE IN OHMS AT 200 OPS

1. R1=2.4K
2. R2,R6=1.2K
3. R3,R7,R8=1K
4. R4=2K
5. R5=1.8K

NOTES:

1. VEE=-5.0VDC
2. ALL TRANSISTORS ARE 2TIL12W4
3. VCC=+5.0 VDC
4. P_D=20mw

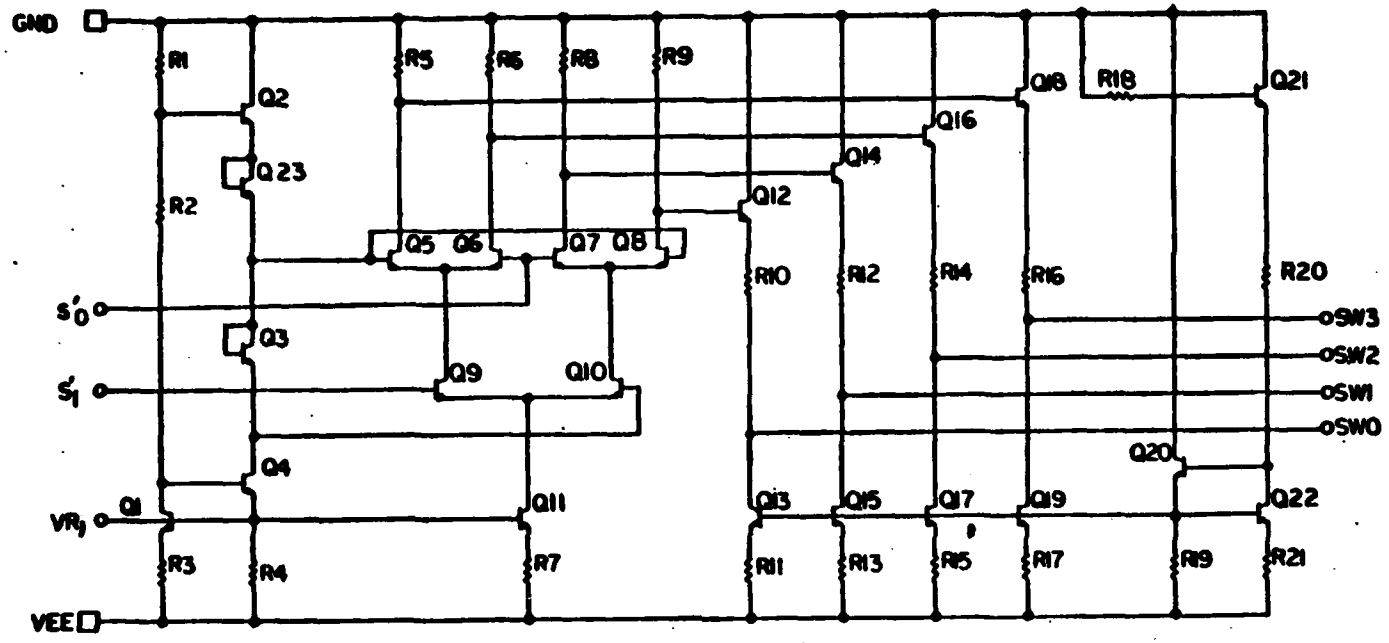


Figure 3-8.
R.F. SWITCH
DECODER AND LEVEL SHIFTER

RESISTOR VALUES ARE IN OHMS AT 200 OPS.

1. R1,R3=600
2. R2=5.28K
3. R4,R19 = 2.4K
4. R5,R6,R8,R9,R18=1200
5. R7=600
6. R10,R12,R14,R16 = 4.66K
7. R11,R13,R15,R17,R21 = 475
8. R20=5.0K

NOTES:
1. VEE=-5.0 VDC
2. ALL TRANSISTORS ARE 2TIL12W4
3. P_D=23.0mw
4.

S_0	S_1	SELECT
0	0	SW0
0	1	SW3
1	0	SW1
1	1	SW2

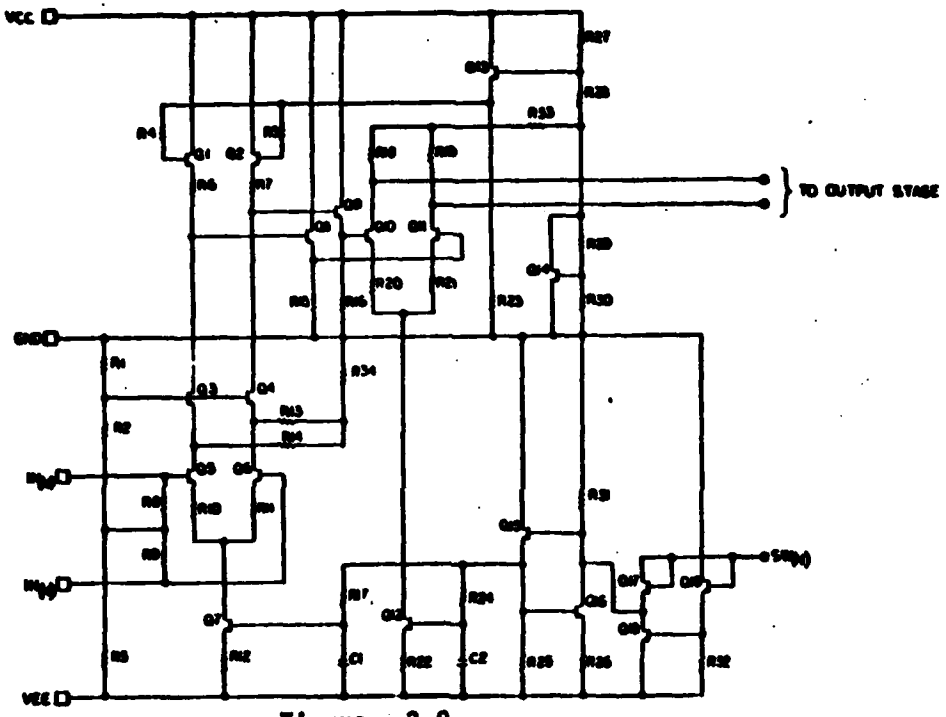


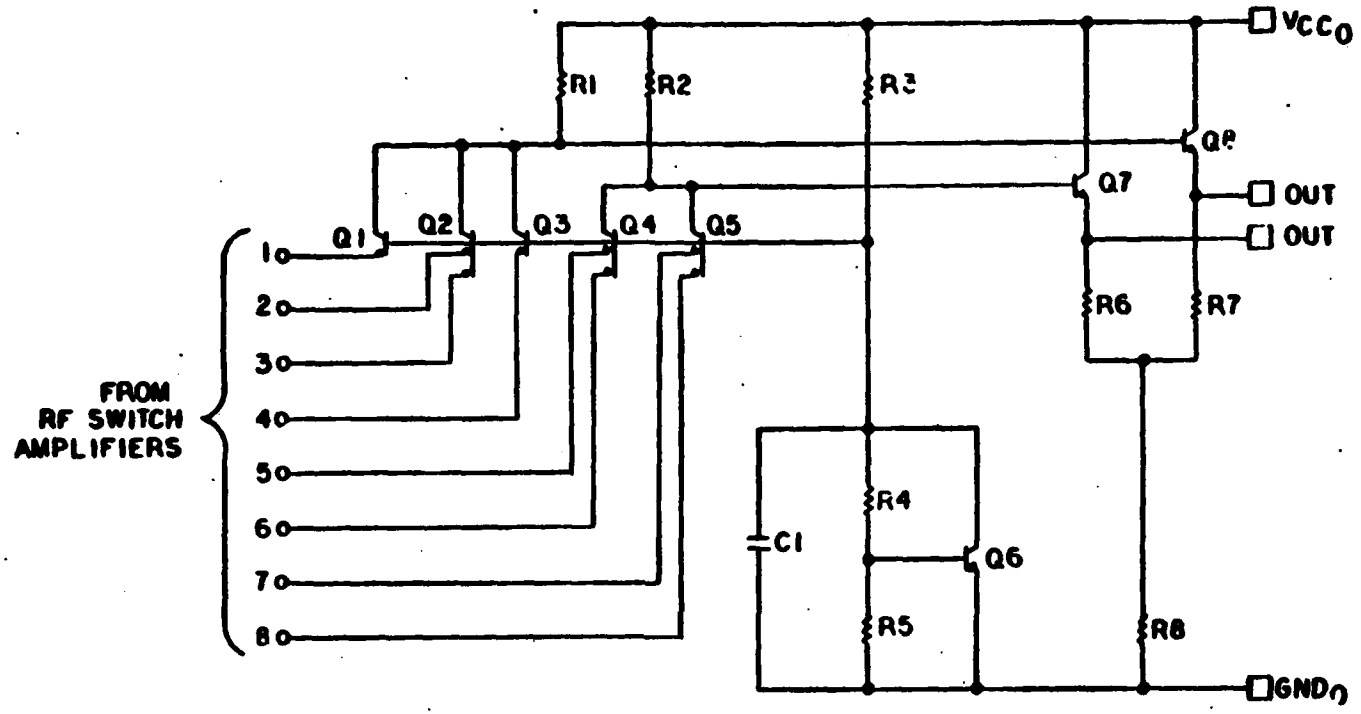
Figure 3-9.

RF SWITCH AMPLIFIER

RESISTOR VALUES in Ohms at 200 MHz

1. R1,R17,R24 = 400
2. R2 = 3.6K
3. R3 = 3.6K
4. R4,R5 = 1200
5. R6,R7 = 250
6. R8,R9,R10,R15,R16,R34=1K
7. R11,R14,R18,R21 = 30
8. R12,R22 = 200
9. R13,R19,R30 = 15K
10. R23 = 4K
11. R25 = 300
12. R26 = 900
13. R27 = 15K
14. R28 = 350
15. R29 = 42K
16. R31 = 5.6K
17. R32 = 16K
18. R33,R34 = 5.0K
19. C1,C2 = 2.4 pf

NOTES:
1. VEE = -5.0 VDC
2. ALL TRANSISTORS ARE 2THU804
3. CAPACITORS ARE BURIED LAYER TO ISOLATION DIODES.
4. VCC = 5.0 VDC
5. INPUT PADS ARE 4 MILS IN DIAMETER.
6. P_D = 57.6 mw



RESISTOR VALUES ARE IN OHMS AT 200 OPS

R1,2=200
R3=1.65K
R4=4.2K
R5,8=1.5K
R6,7=1K
C1=2.0 PF

Figure 3-10.

RF SWITCH OUTPUT STAGE

NOTES:

1. ALL TRANSISTORS ARE 2TIL12W4
2. VCC_0=5.0+VDC
3. CAPACITOR IS BURIED LAYER TO ISOLATION DIODE.
4. OUTPUT PADS ARE 4 MILS IN DIAMETER.
5. P_D=19.6 mw

Extensive computer simulations, using SPICE 2, were performed to investigate frequency performance and temperature stability of the switch. The circuit was simulated in two sections: (1) digital select circuitry; and (2) RF switch amplifier. A transient analysis was used for the digital circuitry, and an AC analysis was performed on the switch amplifier. The computer predicted performance is summarized below in Table 3-5.

Table 3-5. SWITCH COMPUTER PREDICTED PERFORMANCE

Switch Amplifier Voltage Gain	17 dB
Temperature Variation of Gain (-55°C to 125°C)	±1 dB
3 dB Bandwidth	600 MHz
Temperature Variation of Bandwidth (-55°C to 125°C)	±50 MHz
Switch Amplifier ON/OFF Ratio	>70 dB
Digital Select Circuitry Propagation Delay	10 ns
Temperature Variation of Propagation (-55°C to 125°C)	±2 ns

Some comments on the interpretation of computer simulation are in order. A very pessimistic model for the OAT (Oxide Aligned Transistor) device was used in all simulations, therefore it is expected that the computer predictions will be an accurate representation of worst case performance. The gain of the switch amplifier in the OFF state was predicted to be well below -100 dB. This result does not inlcude substrate coupling. The substrate coupling was minimized by careful circuit layout and is not expected to be a problem. Chip size is 71 x 85 mils.

(2) RF/LSI Mix-and-Divide Circuitry

The configuration of the divider/mixer chip suitable for integration is shown in Figure 3-11. The mix-and-divide circuitry is a monolithic IC consisting of a programmable (÷3/÷4) frequency divider, an analog multiplier, and the associated level setting and buffering circuitry. All internal circuitry is differential, so that buffer amplifiers are required on both the input and the output that interface with bandpass filters. The mixer input from the SP4T switch is differential, since the SP4T switch output is differential.

The ÷3/÷4 uses low level differential logic, which interfaces well with the rest of the circuitry. A block diagram of the divider is shown in Figure 3-12. The logic is somewhat unconventional, but allows the counter to be implemented with gates with only two inputs, which permits the full speed capability of the differential logic to be realized. This insures that up to 800 MHz divider operation can be routinely achieved without the need to select chips and possibly suffer a yield loss. The additional AND gate shown on the output is optional; in the ÷3 mode, it provides a 50% duty cycle output rather than the 1/3 or 2/3 duty cycle normally obtained from a ÷3, and thus suppresses the DC and even harmonic components fed to the mixer. Figure 3-13 shows the schematic of the ÷3/÷4 circuit. This circuit utilizes five latches and one AND gate. The divider could be implemented with only four latches, but it is likely that maximum operating speed would be under 800 MHz. Computer simulations of the divider have begun. Emitter follower level shifters that prevent saturation may be necessary in each latch to insure the specified operating frequency. Power dissipation is expected to be in the 150-250 mW range.

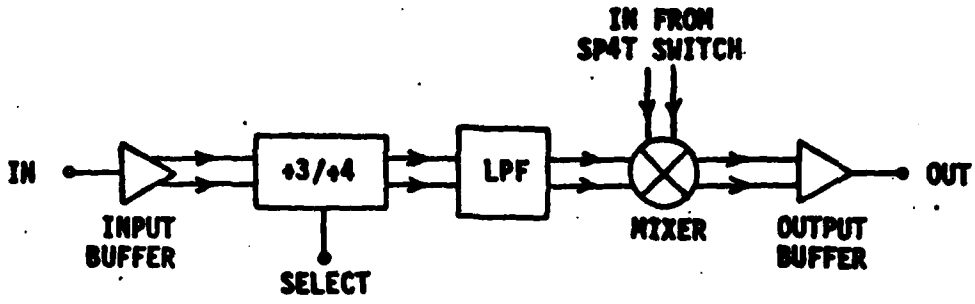


Figure 3-11. Mix and Divide Circuitry

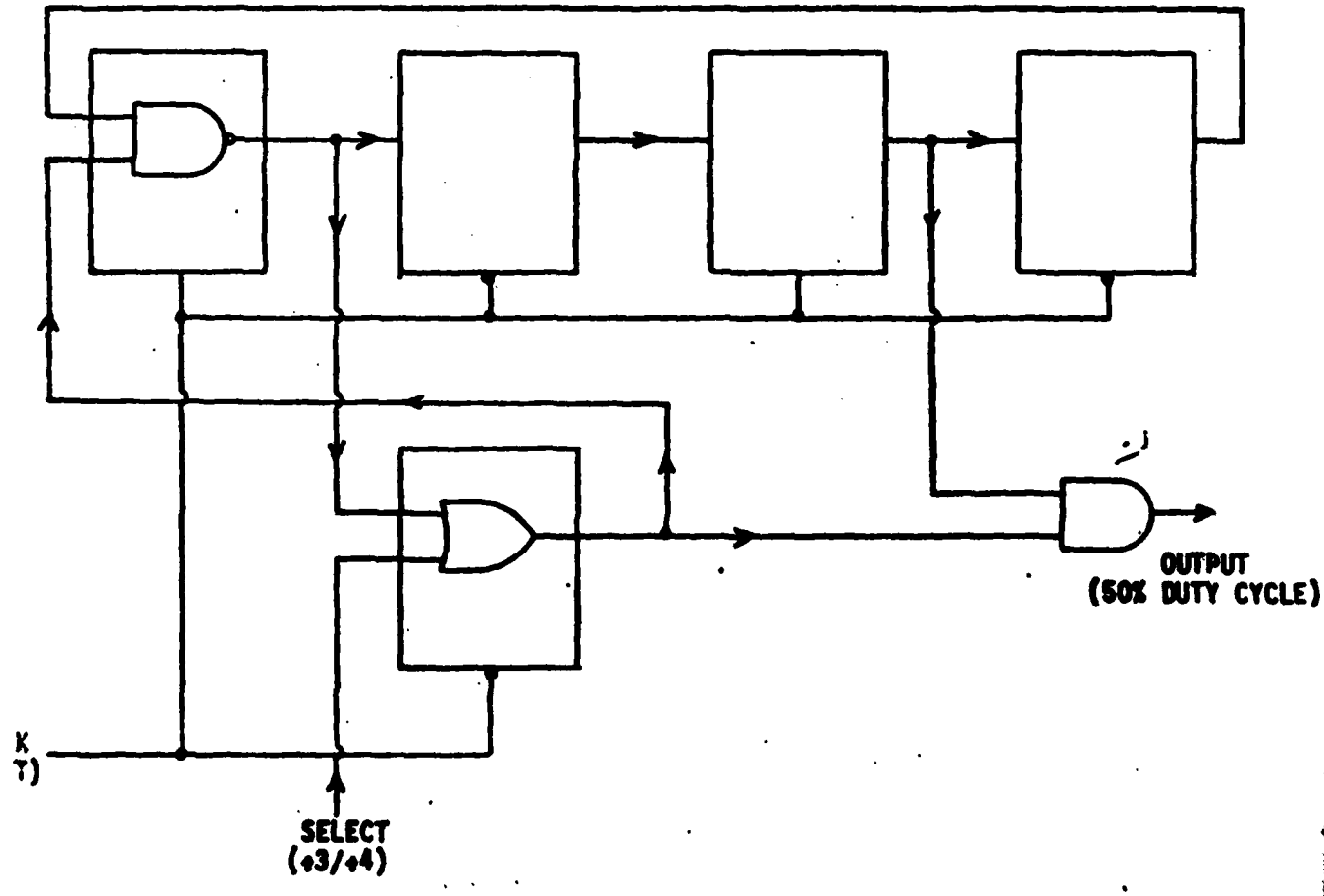


Figure 3-12. ÷3/÷4 WITH 50% DUTY CYCLE OUTPUT

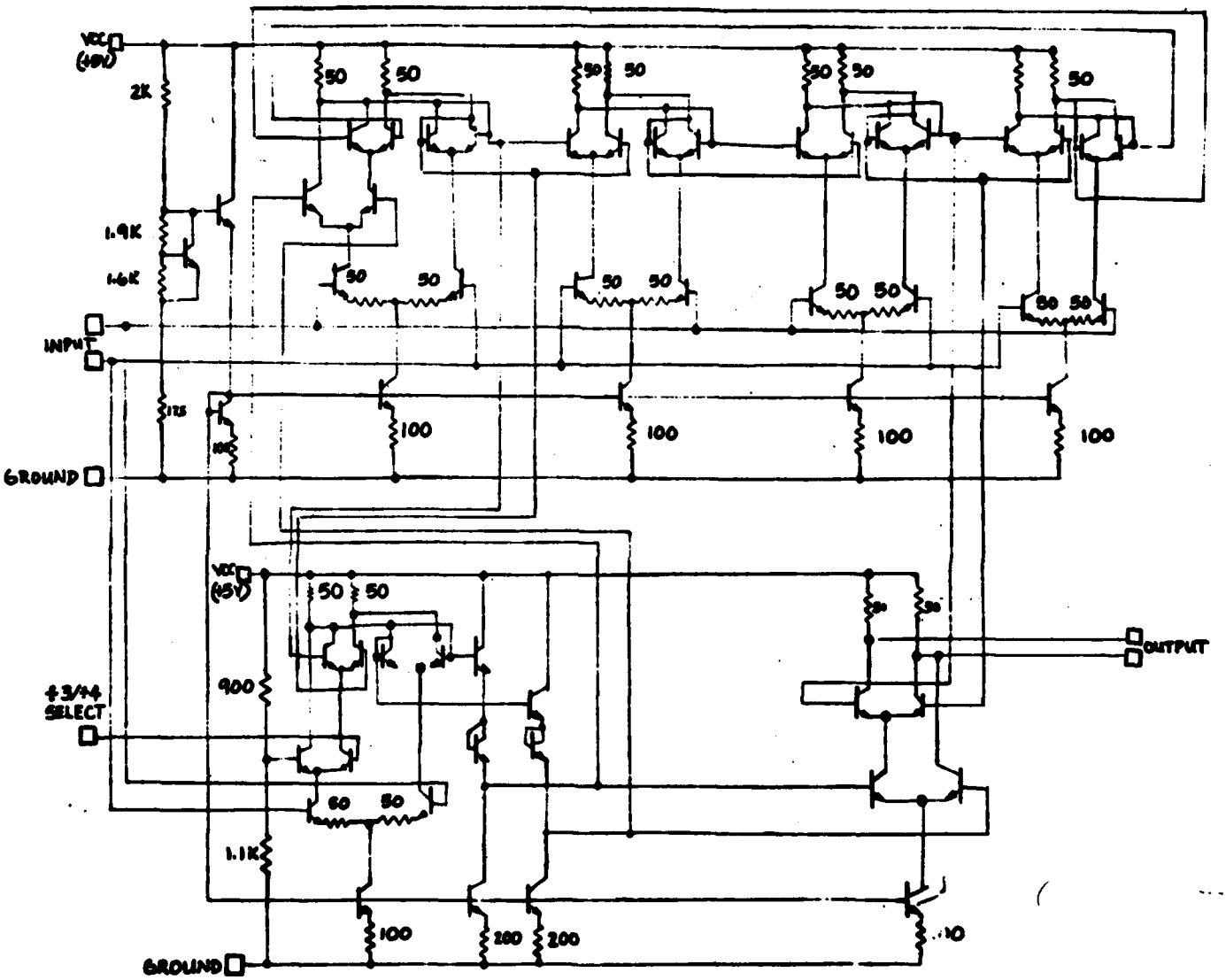
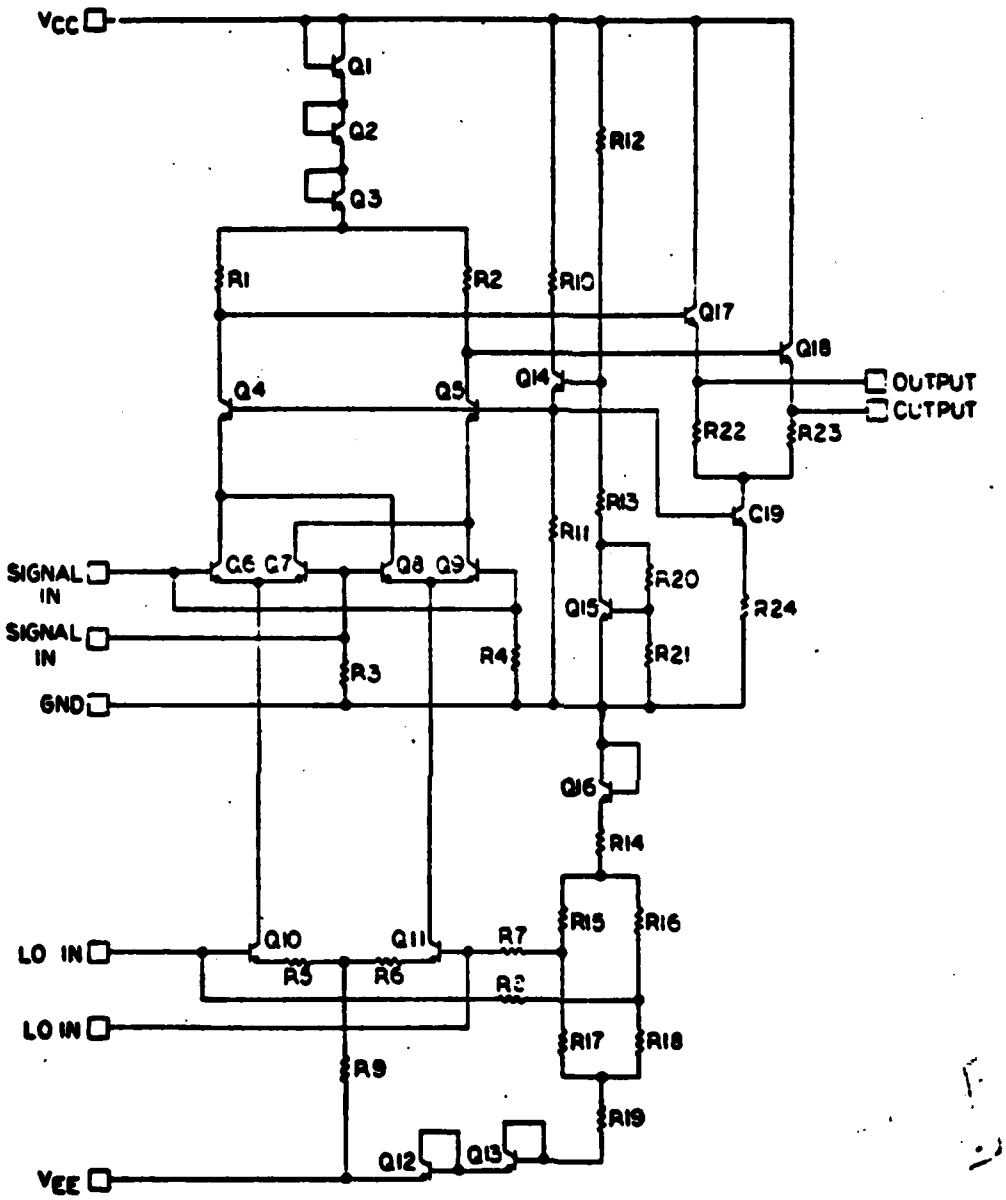


Figure 3-13. ÷3/÷4 Circuit

A schematic of the mixer is shown in Figure 2-14 . This circuit is a variable transconductance four-quadrant multiplier. Similar devices have been built in the past at TRW and a dynamic range of greater than 70 dB is expected from this device.



RESISTOR VALUES ARE IN OHMS AT 200 OPS

R1-6,15-18=100
R7,8=2K
R9=400
R10=3K
R11=5.2K
R12=4K
R13=2.4K
R14=2.5K
R19=1.3K
R20=3.3K
R21=1.5K
R22,23=1K
R24=1.1K

DEVICE TYPES

Q1,2,3,19=2T2L17W3
Q6-Q9,Q12-Q16=2T1L12W3
Q4,5,10,11,17,18=2T2L12W3

NOTES:

1. V_{CC}=+12.0 VDC
2. V_{EE}=-6.0 VDC
3. R15-18 ARE LASER TRIMMABLE (L=3GRIDS+3,COMP, W=6 GRIDS)
4. INPUT & OUTPUT PADS ARE 4 MILS IN DIAMETER.
5. P_D=158 mw

Figure 3-14. Analog Multiplier

4. CONCLUSIONS AND PROJECTED PLANS

The microwave oscillator development is essentially complete. All that remains is the two contractual models. A series of unexpected difficulties was experienced during translation of the breadboard designs into the deliverable hardware units. These problems included:

- o Non-reproducibility of a phase shift through the SAW filters between the breadboard and deliverable units.
- o Oscillations in the loop amplifiers.
- o Non-reproducibility of .5W oscillators.

In addition, a desire was expressed to have one device control the phase shifter. This required experimentation with varactor diodes instead of manually adjustable capacitors. Tests to demonstrate phase shifts were successful with the diodes but temperature compensation to correct for capacitance change due to temperature will be required. At this time, all the technical issues appear to be well-defined and no further problems are anticipated. Delivery of the two units is expected by January 1980.

The synthesizer architecture was revised following experimental investigation of the MLSO. An alternate design has been completed. Fabrication of the RF/LSI chips are well underway and design of the SAW filters and oscillators has begun.

During the next reporting period (after delivery of the oscillators), the synthesizer phase of the program will be addressed. Tasks which will be accomplished include:

- o Breadboard and prove out the revised design for the frequency sources in the synthesizer.
- o Begin tests and characterization of the RF/LSI chips.
- o Complete the design of the SAW filters and oscillators.
- o Fabricate the SAW devices and test their performance.

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